

AccuCore

Release Notes

11/04/11

RELEASE NOTES

VERSION 2.4.42

ALTERATIONS AND ENHANCEMENTS

- Improve path tracing performance and timing arc analysis calculations

VERSION 2.4.41

ALTERATIONS AND ENHANCEMENTS

- Adjust STA engine flattening and instance names recognition
- Change backannotated nets count calculation to match method of counting total nets

VERSION 2.4.40

ALTERATIONS AND ENHANCEMENTS

- Embed CatalystDD Verilog flattening and bus expansion utility into STA netlist engine

VERSION 2.4.39

ALTERATIONS AND ENHANCEMENTS

- Extend Verilog and DSPF netlist bus syntax handling in backannotation process

VERSION 2.4.37

ALTERATIONS AND ENHANCEMENTS

- Speed up STA path analysis when using DSPF netlist RC backannotation data

VERSION 2.4.35

ALTERATIONS AND ENHANCEMENTS

- Change SDF model generation to provide all black box model paths on outputs and not only worst paths

VERSION 2.4.34

ALTERATIONS AND ENHANCEMENTS

- Expand Verilog syntax checking for wire statements during pre-processing phase to report errors in malformed input netlists

VERSION 2.4.33

ALTERATIONS AND ENHANCEMENTS

- Perform Verilog pre-processing checks and autocorrect basic input syntax violations to allow processing to continue when able
- Extend ADD_CELL_TYPE processing of Verilog instance names to ALL cells requiring this data

VERSION 2.4.32

ALTERATIONS AND ENHANCEMENTS

- Change multiple defined hierarchical ports names handling from errors to warnings and permit processing to continue
- Improve remaining STA Verilog multi-line statement processing to ignore simple syntax errors and continue
- Extend Liberty .lib processing for minimum pulse width statements to support 2D slope tables
- Adjust Verilog generation and SPICE input netlist refdes name handling when processing .cfg file SUBCKT_BLACKBOX and SUBCKT_KEEP statements
- Improve error and warning reporting messages to be more descriptive and provide basic corrective action recommendations

VERSION 2.4.30

ALTERATIONS AND ENHANCEMENTS

- Improve high priority STA Verilog multi-line statement processing to ignore simple syntax errors and continue

VERSION 2.4.29

ALTERATIONS AND ENHANCEMENTS

- Adjust SPICE netlist instance handing for resistors and diodes to match SmartSpice supported syntax variations
- Extend X-call and "/" character SPICE netlist processing to match SmartSpice supported syntax variations
- Improve Verilog and Liberty .lib generation for .cfg files with SUBCKT_KEEP statements to track instance name cross references and preserve input naming in lieu of auto-created naming

VERSION 2.4.28

ALTERATIONS AND ENHANCEMENTS

- Adjust SPICE netlist instance name handing of auto-created cells

VERSION 2.4.27

NEW FEATURES

- USE_X_CALLS option to control including or excluding "x" in instance names when processing DSPF files

ALTERATIONS AND ENHANCEMENTS

- Change hierarchical separator default behavior processing for "/" character

VERSION 2.4.24

ALTERATIONS AND ENHANCEMENTS

- Extend SIMULATE_SCCS to permit processing cells attached to block outputs
- Extend BDD processing for complex structures and update error reporting for cells that fail function screening checks
- Modify DSPF file processing for ground nets named GND

VERSION 2.4.21

ALTERATIONS AND ENHANCEMENTS

- Adjust STA delay calculation processing for cells with rise/fall transitions that occur prior to 50% measurement input edges (negative delays)

VERSION 2.4.19

ALTERATIONS AND ENHANCEMENTS

- Improve DSPF processing of primary output naming, busbit handling, hierarchical separator processing, *|NET name cross-referencing, coupling capacitance processing and resistor subnet tracing
- Change SPICE netlist cell instance connectivity tracing across hierarchical boundaries
- Extend Liberty .lib to netlist bind operations to account for variations in cell port/pin counts of different instances of the same cell with empty pins as per Verilog IEEE standards
- Extend Liberty .lib processing to support 2D tables for minimum pulse width data types
- Improve case sensitivity handling during backannotation in STA
- Extend Verilog netlist processing of ({...}) style pins definitions

VERSION 2.4.18

ALTERATIONS AND ENHANCEMENTS

- Change circuit characterization measurement communication method for hold timing
- Improve DSPF net names processing for long names
- Improve STA analysis method when processing derived clocks
- Adjust DSPF files processing for GLOBALS declarations
- Change dir-path location processing for .tbl table vector files to avoid file naming collisions

VERSION 2.4.15

ALTERATIONS AND ENHANCEMENTS

- Improve FAST_MODE import error reporting to be more descriptive and suggest corrective action

VERSION 2.4.14

ALTERATIONS AND ENHANCEMENTS

- Modify function extraction to permit processing to continue when isolated input errors are encountered on complex cell structures
- Extend SDF file generation syntax to include multiple timing arc calculations

VERSION 2.4.13

ALTERATIONS AND ENHANCEMENTS

- Adjust SDF delay calculations to include results from multiple timing arcs

VERSION 2.4.11

ALTERATIONS AND ENHANCEMENTS

- Modify STA DSPF backannotation to permit processing to continue when isolated input errors are encountered

VERSION 2.4.10

ALTERATIONS AND ENHANCEMENTS

- Extend STA DSPF processing capacity of boundary pins, RC elements and instances to better handle large designs

VERSION 2.4.9

ALTERATIONS AND ENHANCEMENTS

- Extend STA report_warnings to include max_capacitance attribute design rule violation analysis
- Improve RC parasitic netlist processing accuracy and performance for FAST_MODE
- Improve RC parasitic netlist processing for large power and ground nets
- Improve RC parasitic netlist processing for SDF timing generation
- Adjust Verilog and SPICE netlist output port instance name matching when multiple connection types exist
- Adjust input pin capacitance characterization method for pass gate style cells
- Modify OUTPUT_LVS_NETLIST 2 mode RC tree trimming method
- Change net name handling for pattern based net processing with FIND_BLACKBOX