

New Features Facilitate DRC Clean Layout and Parasitic Effect Debugging

Introduction

When it comes to delivering IC design, time to market and first pass success are very important factors. Layout verification (DRC) and parasitic effect estimation are both time consuming and can have a direct impact on these two factors. Our new ICCAD suite release has new features allowing the layout designer to speedup the delivery of DRC clean layout with proper parasitic effect considered. This application note will describe these features and their uses.

Faster DRC Clean Layout

In an effort to assist the layout designers to deliver DRC clean layout in a shorter time, a new feature was added to our Expert layout tool. The technology file (*.tcn) can now store some DRC rules that will be checked during the geometries edit operation. The rules currently implemented are: Min Width, Min Space, Min Space between Layers, Min Overlap, Min Enclosure and Min Notch. These rules can be setup for every drawing layers listed in the technology file.

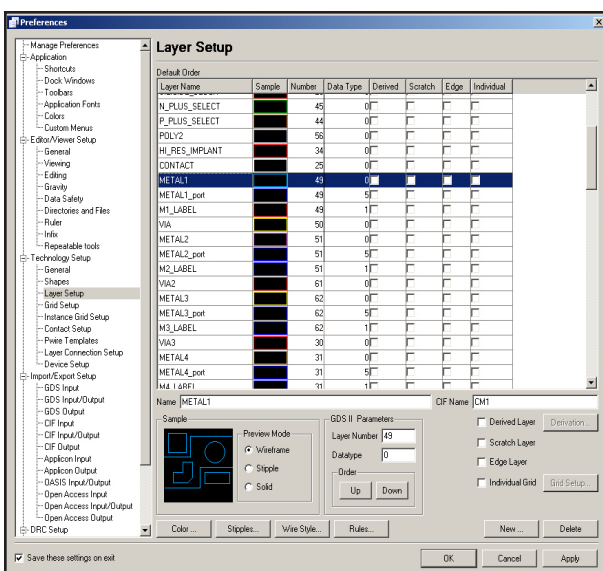


Figure 1. Layer Setup window.

In order to access these rules, the following sub-menu in the Expert Layout tool needs to be selected: Setup>>Technology...>>Layer Setup... Figure 1 illustrates the Layer Setup window.

After selecting the layer of interest (METAL1 in this case) the “Rules...” button, located in the lower part of the window, needs to be pressed. A new window, allowing the access to the different rules, opens as shown in Figure 2. When the setup of the different rules is completed, pressing OK accepts the setting; the Layer Setup window also needs to be closed by pressing OK before these rules can take effect.

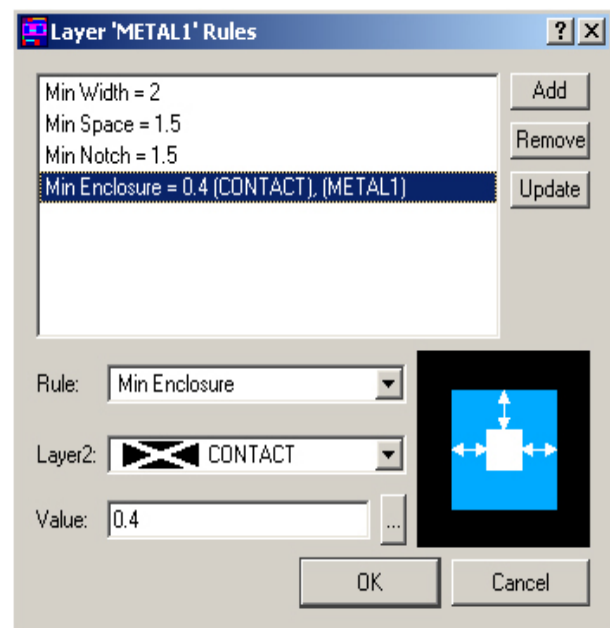


Figure 2: Rules... setup window for METAL1.

After completion of the Rules... setup, the user will notice that during geometries edit or modification, a small red arrow will appear if a rule is being violated. Figure 3.a and 3.b illustrates violation of a Min Space (set to 1.5um) and a Min Enclosure' (set to 0.4um) rule respectively.

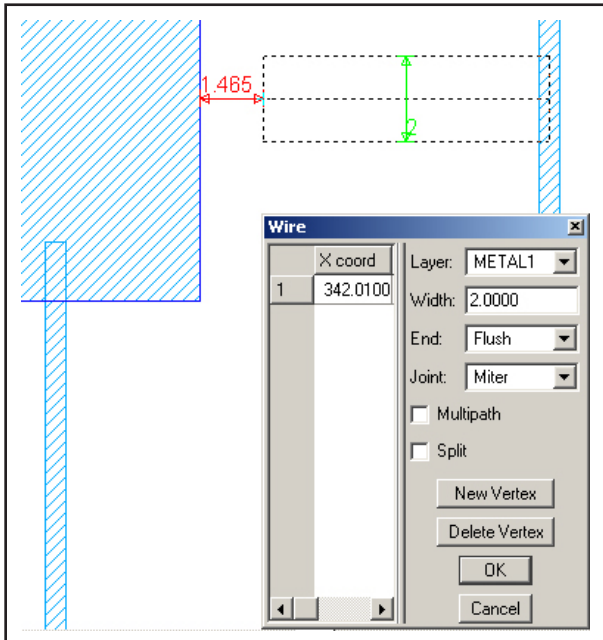


Figure 3a: Min Space Violation.

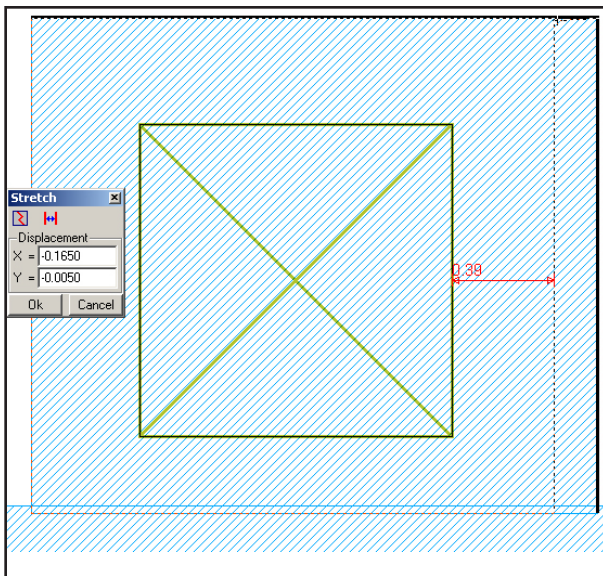


Figure 3b: Min Enclosure Violation.

Once the geometries edit is completed, the red and green arrows disappear, as it is assumed that the user wanted to maintain this placement, regardless of the violation. Additionally, the rules can be set to consider the geometries located at the same level of hierarchy only or at other levels of hierarchy, including the geometries located in lower level instances. Specifying the level of visibility through the use of the Expert submenu View>>Cell View>>Hierarchy Depth will alter the amount of data being considered by the rules. The geometries being considered are basically the one visible in the layout view.

It should be noted that, in addition to these rules, the “RealTime DRC” feature can also be setup to run other DRC checks at the completion of the edit operation. See the Expert design manual for more information on the “RealTime DRC” feature.

Parasitic Effect Debugging

A second interesting feature that was added to the IC-CAD tool set, is the ability to node probe the layout after parasitic extraction, in order to measure the parasitic resistance between two chosen points or the parasitic capacitance of a specific net. In this section, it is assumed that the reader knows the steps to generate a netlist including the parasitic effect of the layout. The following application note, describes in detail these steps: http://www.simucad.com/content/appNotes/iccad/2-010_Parasitic_back_annotation.pdf.

Often, the circuit designer is fully aware of the critical paths/nets of its design. As of now, the simulation of the post layout parasitic back-annotated netlist was the recommended approach to estimate the silicon behavior of the physical design. Based on the post layout simulation results, the designer could do the required modifications to the layout to ensure proper functionality of the design. However, in the previous flow, finding the parasitic effects to modify could be laborious. This new version of Expert (4.5.15 and newer) simplifies this task considerably.

In order to have all the required information to measure the capacitance and resistance of nets, the DSPF option needs to be selected during the RC parasitic extraction. In the Expert submenu Verification>>Extraction>>Setup under the section Netlist, the option “Generate DSPF file” needs to be checked. (See figure 4)

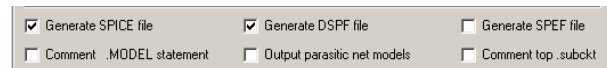


Figure 4: LPE setup, Netlisting section.

On completion of the parasitic extraction netlist, the user can view the netlist by selecting the Open Netlist button, as shown in figure 5. In order to measure the point-to-point parasitic resistance and the net capacitance, the node of interest needs to be highlighted using the Node Probing tool located in the Expert submenu Verification>>Node Probing>>Pick Node. Figure 6 illustrates the highlighted node using the node probing tools; the total net capacitance to ground of this net is estimated to be 0.181315 PF.

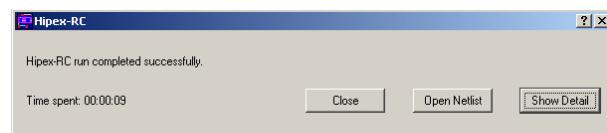


Figure 5: Open Netlist option.

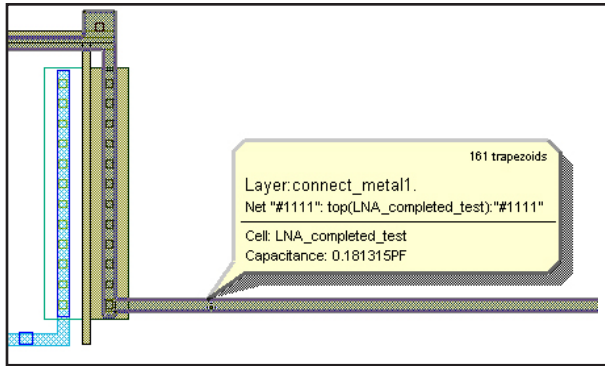


Figure 6: Net Capacitance.

To measure the point-to-point parasitic resistance of the highlighted net, the user needs to left click with the Node Probing tool, while holding the CTRL key, the two locations between which the resistance needs to be known. On completion of the second click, the tool reads the DSPF database and finds the closest sub-nodes to the user defined points. Two small crosses will identify the sub-nodes chosen by the tool. The effective resistance is then calculated using the delta-Y transformation of resistance network. Figure 7 displays a value of 1.8669 Ohm for the portion of the net selected.

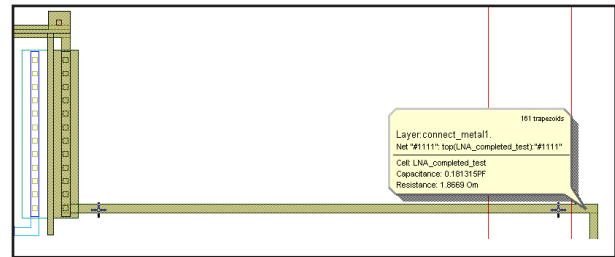


Figure 7: Point-to-point resistance.

Conclusion:

This application note has described two new features to facilitate and speedup the delivery of DRC clean layout and the debugging of parasitic effect. Many other features, not discussed in this application note, were added to this new release of the ICCAD tool suite. The reader is invited to consult the release note to learn more about the new additions.