

High Accuracy Capacitance Extraction of the Delta Type PIXEL Using CLEVER

Introduction

The pressure to reduce the manufacturing cost of TFT LCD displays is constant and intense. Today, critical issues in the processing of TFT arrays include the development of a low-resistance gate-bus line, uniform and fine etching, and improved lithographic accuracy. TFT-array technologies aim to achieve high precision, large aperture ratio, and low power consumption, in addition to large screen size.

Also, the fabrication of the color filters (CFs) is an important manufacturing issue. Color filters can be made with either dyes or pigments, utilizing coloring method such as dyeing, diffusion, electro-deposition, and printing. The color mixing method is important for getting the high color mixing. In general, there are 3 types for the color mixing, the most popular stripe-type, mosaic-type and delta-type. The delta-type is the best color mixing method on LCD displays to get the high resolution.

In this article, CLEVER shows the accuracy of the Capacitance between ITO and signal metal lines, and the capability to study of the structure dependence[1].

Flat-Panel Display and CLEVER

The 3D process models within CLEVER allow the geometry of the final structure to be generated once all the back end process phases are performed. These include the deposition, etching and lithography through the GD-SII layout patterns. CLEVER also considers the aspect ratio which is the mesh quality of the active TFT device and large pixel region.

For the color mixing, there are 3 types as in Figure 1.

The Stripe-typed is currently the most popular, but the Delta-typed has the best color mixing capability and each sub-pixel can turn on or off independently so that the pixel edges will become finer for the same panel size and resolution.

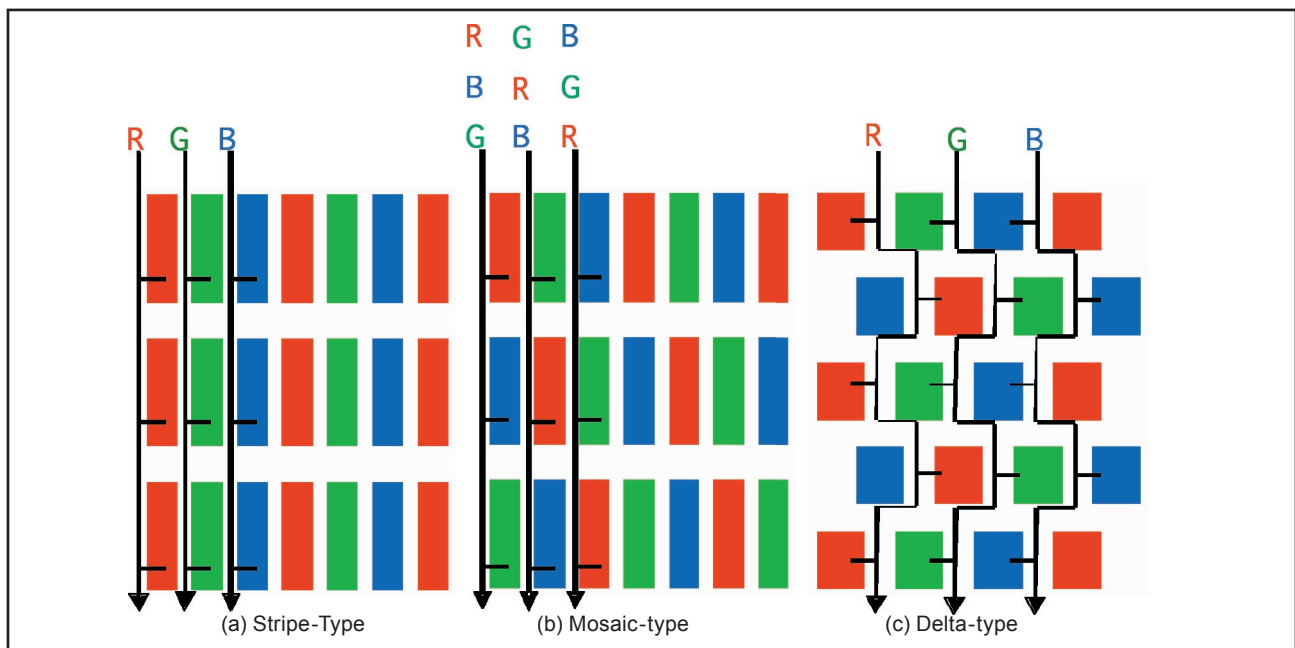


Figure 1. Panels sub-pixels arrangements. (a) Stripe-typed (b) Mosaic-typed and (c) Delta-typed.

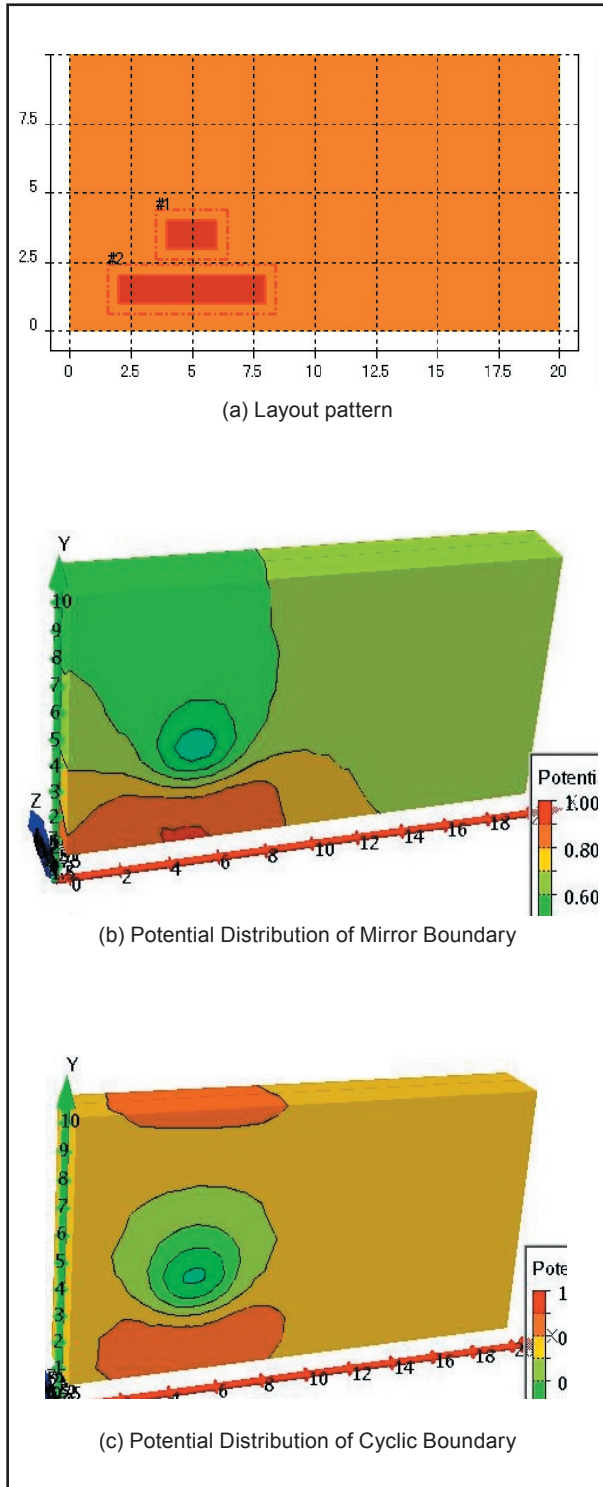


Figure 2. Layout pattern and potential distribution due to boundary condition.

(a) Layout pattern and potential distribution of (b) Mirror Boundary

(c) Cyclic Boundary

To get the accurate parasitic Capacitance of the Delta-typed pixel, CLEVER successfully makes the symmetric mesh and cyclic boundary condition. Delta-typed makes it most difficult to predict the parasitic Capacitance on the 3 types of pixel.

Figure 2 shows the potential distribution dependency on the boundary condition, for cyclic and mirror boundary conditions. The Delta-typed pixel should be selected the cyclic boundary condition.

Capacitance and Delta PIXEL

From these conditions, the delta-type pixel pattern has a 3 color signal line, and 11 panel was chosen to simulate as the unit pattern. To compare the RGB signal line and ITO pattern, the capacitances are chosen from the all the patterns.

The accurate parasitic Capacitance is shown in Figure 3.

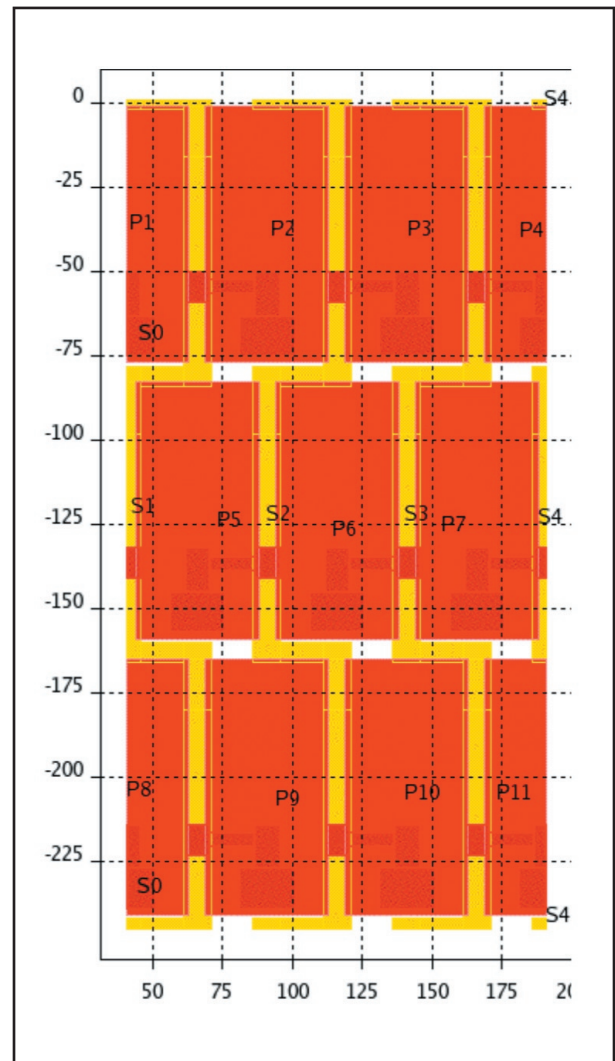


Figure 3a. Delta-type Pixel Layout Pattern.

P2-P3	8.8183417e-16
P5-P6	8.7936163e-16
P6-P7	8.7802546e-16
P9-P10	8.8225600e-16
P2-P5	2.7449851e-16
P5-P9	2.7371048e-16
P3-P6	2.7329723e-16
P6-P10	2.7419368e-16
S1-P2	1.1852842e-14
S1-P9	1.1800253e-14
S2-P3	1.1885243e-14
S2-P5	1.1825975e-14
S2-P10	1.1853127e-14
S3-P6	1.1826391e-14

Figure 3b Capacitances Groups.

Here the S1, S2, S3 is the RGB signal line and from the P2 to P10 is the RGB color panel. The Panel P2 and P3, P5 and P6, and P9 and P10 should be same capacitance. And the P2 and P5, P5 and P9 should have the same capacitance. And finally, each of the RGB signal lines and panels should have same capacitance.

In Figure 3, those 3 Groups have the same capacitance and the distribution of the capacitance values compared of each groups has the lower than from 0.6% to 1.2%. This ensures the high accuracy of mesh generation during extraction simulation and symmetric mesh generation as well.

Conclusion

An accurate 3D Field Solver with symmetric mesh in CLEVER can be applied to TFT-LCD with Delta-typed Pixel panel design to predict the Capacitances between the RGB signal line and panel.

The process variation such as the deposition thickness or etching depth and also pattern width is easily simulated with process model and layout connection in CLEVER. This demonstrates CLEVER’s ability to provide good FPD design configurations.

Appendix

[1] Application Note 2007-005, Simucad