

# SmartSpice Analog Circuit Simulator



SmartSpice Overview



**SIMUCAD**



## SmartSpice Background

- Development started in 1986 with 3A1; incorporated major changes and standardized software development on coding rules of 3C.1 and 3D.2 releases
- Objective - complete solutions to Analog Circuit Simulation requirements
- True C/C++ language architecture to take advantage over other vendors still based on FORTRAN language
- Final product has the advantage of being compatible with standard Berkeley SPICE syntax and data structures



## SmartSpice Background (con't)

- Rapid acceptance as the industry standard worldwide
- Large customer base
- All major companies have a copy of SmartSpice
- Broad spectrum of users from individuals and Startups to large multinationals.



## Problems in Analog Circuit Simulation:

- Poor model quality for existing technologies and non-existing models for emerging new technologies (FRAM, SOI, TFT, HBT, etc)
- Poor convergence and speed
- Poor numerical accuracy
- Monolithic code prohibits easy custom model development
- PC Unix & Linux compatibility problems
- Compatibility problems between different simulators (models functionality and netlists)
- Poor customer support
- Integrated with CAD tools but not with extraction, statistical and TCAD tools



## Objectives

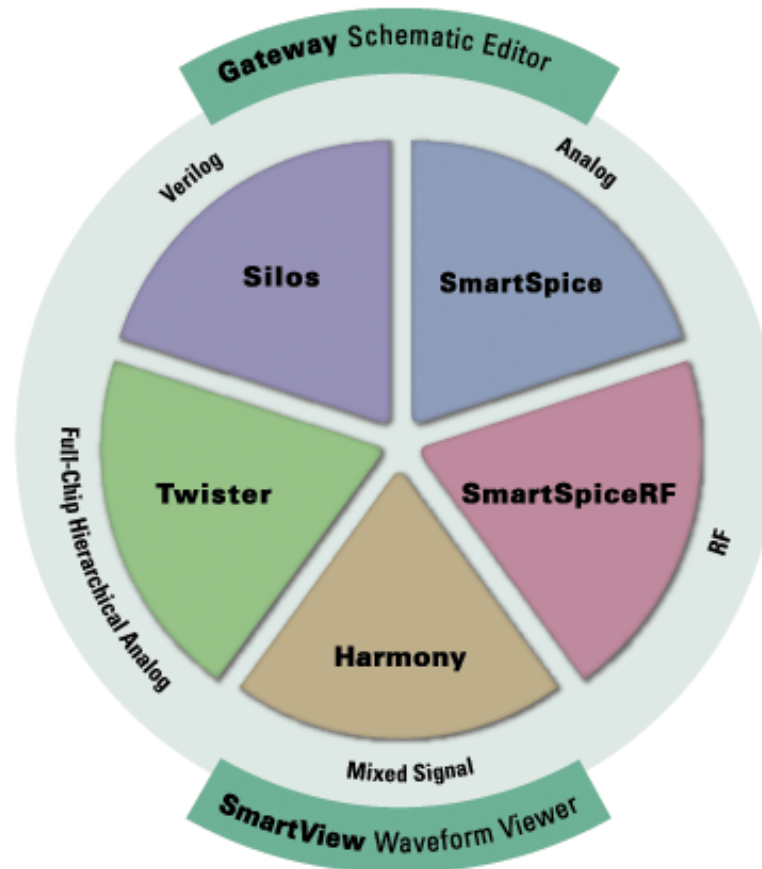
- Revolutionize Analog Simulation market by providing:
  - better proven products
  - better flow integration
  - better support
  - Better set of models with quick implementation
  - better price



## Solution: SmartSpice

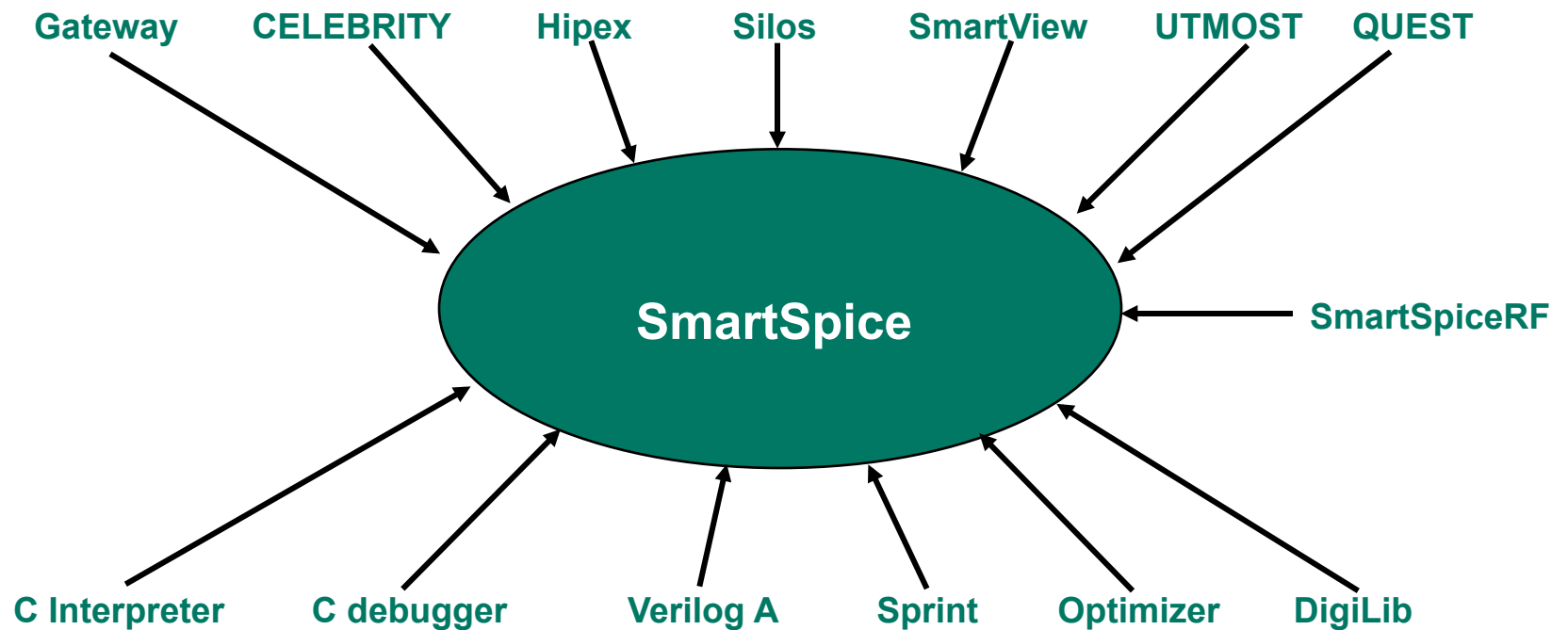
- Fast, robust and easy-to-use analog circuit simulator
- Provides industry leading device model technology coverage, simulation speed, convergence and accuracy
- HSPICE™ compatible input decks and translation from the major SPICE products PSPICE™, ELDO™ and Spectre™ with minimal changes
- Has advanced features such as SmartView waveform viewer, interactive run control and industry leading parametric analysis features
- A user friendly interactive interface as well as a batch mode enable both the novice and the experience user to get the maximum from the tool

# SmartSpice as a Key Member of Complete Simulation Solution



# Integration within Simucad Product Line

- SmartSpice is integrally integrated with a number of Simucad products





## SmartSpice Analysis Techniques

- DC Analysis
- AC Small Signal
- Transient Analysis
- Transfer Function
- Network Analysis
- Sensitivity Analysis
- Noise Analysis
- Transient Noise Analysis
- Distortion Analysis
- Fourier Analysis
- Forward/Reverse FFT
- Monte Carlo Analysis
- Worst-Case Analysis
- Pole-Zero Analysis



## Convergence and Speed

- SmartSpice provides superb convergence and speed because of:
  - Advanced convergence algorithms
  - Initial points algorithms
  - Options and advanced timestep control algorithms to speed up simulation
  - Model continuity
  - Comprehensive problem diagnostics
- Customer benchmarks have demonstrated 8 times speedup over other major circuit simulators for large circuits containing many thousand transistors



## Convergence and Speed: Convergence Algorithms

- DC convergence is based on proprietary stepping algorithms developed by Simucad
- The option CONV=5 (default) helps the Newton-Raphson method to find a solution starting from (typically) zero initial conditions
- To achieve DC convergence it automatically selects one of the following advanced stepping algorithms:
  - GMIN stepping
  - DiagGMIN stepping
  - DCGMIN stepping
  - Source stepping
- The proprietary Transient Ramping Algorithm is used in the most difficult cases to compute steady state solution



## Convergence and Speed: Initial Point Algorithms

- The parameters `SAVEV` and `CALLV` are used to store and to retrieve the bias point information from the operating memory. Using the previously computed bias point as the initial condition significantly accelerates DC convergence
- The `.SAVEBIAS` and `.LOADBIAS` statements are used to store and retrieve the bias point from a file
- The continuation `.SAVEBIAS` and `.LOADBIAS` statements can be used to restart a new transient analysis at any point



## Convergence and Speed (con't)

- Convergence
  - Superior convergence is achieved through much better set of solvers and numerical techniques and much better models resulting from years of R&D
  - Large and complex circuits are easily handled with SmartSpice
- Speed
  - Superior speed against all other Spice vendors for single CPU simulation even before introducing parallelization



# Parametric Analysis Statements

- What is Parametric Analysis?
  - Parametric analysis commands allow the user to completely characterize the behavior of the circuit by varying the IC fabrication and operating environment parameters
- Why is it important?
  - Creates an environment in which users can rapidly change parameters and test conditions to stress designs under real-life conditions. This insures the reliability of the circuit design over the operating space



## Parametric Analysis Statements (con't)

- Any device or model parameter can be printed, plotted or measured
- Any device, model or output statement can be parameterized using parameter labels defined by the user in .PARAM statements, on .SUBCKT and X-Cell lines. Parameter labels and parametric expressions can be used anywhere in the input deck
- Any device or model parameters can be modified by parametric analysis commands during simulation
- The reserved parameter label M can be used to specify devices or subcircuits connected in parallel
- Any voltage or current vector, any device or model parameters can be measured by .MEASURE statement



# Parametric Analysis Statements

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## 1 - Global Parametric Analysis Commands:

- SmartSpice supports global and local parametric analysis statements. Parameter modifications made by a global command are applied to the entire input deck. Global parametric analysis commands are:
  - .MODIF - Parametric Analysis Statement
  - .ALTER - Alter Input Deck Statement
  - .TEMP - Temperature Statement



## Parametric Analysis Using SmartSpice: Parametric Analysis Commands (con't)

- Local commands are locally applied to certain analysis statements such as .TRAN, .DC or .AC. Local parametric analysis commands are:
  - .MC - Monte Carlo Analysis
  - .WCASE - Worst-Case Analysis
  - SWEEP - Nested Sweep can be used with the local MODIF (DATA) parameter sets



## .MODIF Statement

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- The .MODIF statement is the most powerful parametric analysis statement in SmartSpice
- This statement can simultaneously and independently modify any device, model parameters, user-defined parameters, temperature and control options
- It terminates the parameter modification process when the user defined stop conditions are satisfied
- Monte Carlo analysis can be performed by the .MODIF statement using 8 types of built-in distribution functions



## .MODIF Statement (con't)

Example on using .MODIF :

```
.MEASURE TRAN DELAY_OUT WAVE V(OUT)
.MODIF RC1(RES) = 2K CLOAD(CAP) = 0.5PF
+ MODIF LOOP =9 STOP DELAY_OUT LE 1.3ns
+ RC1(RES) * = 0.9 CLOAD(CAP) * = 0.95
```

- SmartSpice performs nine or fewer iterations
- In the first iteration it sets the parameters RES to 2K and CAP to 0.5pF
- On each of the following iterations, it multiplies RES by 0.9 and CAP by 0.95 until the measured value DELAY\_OUT is less than or equal to 1.3ns



## .ALTER Statement

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- The .ALTER statement is used for modifying and reloading the input deck several times to
  - alter the model libraries,
  - alter or modify subcircuit definitions,
  - add new analysis commands,
  - modify or add new output statements,
  - modify or add new parameter labels,
  - modify parametric analysis commands,
  - modify or add new control options.
- The .ALTER statement is particularly efficient in conjunction with the .MODIF statement

## .ALTER Statement (con't)

- Example using .ALTER:

```
-  
-  
-  
m1 1 2 0 4 NMOS1 I=20u 25u  
-  
-  
-  
.ALTER  
m1 1 2 0 4 NMOS1 I=16u 25u
```

- The input deck is loaded twice and two circuits are created
- Two output files are created



# Parametric Analysis Statements

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## 2 - Local Parametric Analysis Statements:

- Local commands are locally applied to certain analysis statements such as .TRAN, .DC or .AC.
- Local parametric analysis commands are:
  - .MC - Monte Carlo Analysis
  - .WCASE - Worst-Case Analysis
  - .ST - Nested sweep can be used with the local MODIF (DATA) parameter sets



## Parametric Analysis Using SmartSpice: Local Parametric Analysis Commands

- The .MC and .WCASE commands perform statistical and worst/best case analyses on the circuit for the specified analysis type
- The device tolerances of ALL and EACH types are defined in .MODEL parameter specifications
- EACH independently varies model parameters for each device of the specified model (correlation 0)
- ALL generates the same parameter values for all devices of the model (correlation 1)



## Parametric Analysis Using SmartSpice: .MEASURE Statement

- The .MEASURE statements are used to calculate important circuit characteristics such as delays, rise and fall times, trip and cross points, periods of oscillations, etc.
- Every .MEASURE statement produces only one scalar number that is stored under a user-defined name. Once computed the measure results can be referred to in subsequent .MEASURE statements
- .MEASURE statements can contain arbitrary parameter and vector expressions



## Parametric Analysis Using SmartSpice: .MEASURE Statement (con't)

- Some measurement types are listed below:
  - MAX, MIN                      Maximum, Minimum,
  - WAVE                              Rise and Fall Time
  - DELAY (TRIG)                      Delay
  - CROSS (WHEN)                      Cross
  - ERR, ERR1                      Errors
  - AVG, RMS                      Average, Root Mean Square
  - EXPR (PARAM)                      Parametric Expression



## Parametric Analysis Statements: Conclusion

- Parametric analysis environment in SmartSpice allows the user to be time-efficient because it shortens design cycles. It also insures design reliability by using efficient methods to evaluate the circuit under user-defined conditions



## .ST Statement

- The nested SWEEP command is locally applied to the analysis statement where it is specified
- The nested SWEEP specification can reference a parametric inline .DATA statement
- A .DATA statement can contain an arbitrary number of sets of parameter values



## .ST Statement (con't)

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- Example:

```
.ST DEC QNL(BF) 10 100 10
```

- The parameter BF is swept logarithmically from 10 to 100 with a step of 10 points per decade



## Monte Carlo Analysis

- The .MC and .WCASE commands perform statistical and worst/best case analyses on the circuit for the specified analysis type
- Monte Carlo analysis can be performed using the .MODI F statement and the .MC statement:
  - Using the .MC statement, Monte Carlo analysis will only be performed on model parameters with user-defined tolerances
  - The .MODI F statement will perform Monte Carlo analysis on parameters defined on the .MODI F statement line, and on model parameters with user-defined tolerances



## Monte Carlo Analysis (con't)

- Tolerances for each device or all devices can be defined in the .MODIF statement
  - ALL generates the same parameter values for all devices of the model (100% correlation)
  - EACH independently varies model parameters for each device of the specified model (0% correlation)



# Command Scripts



- The syntax for a command script is:

```
Explanatory Title
```

```
.CONTROL
```

```
<SmartSpice commands>
```

```
.ENDC
```

- The body of the script can contain any command including calls to other script files
- Script files use the same syntax as C-shell scripts
- Supported structures include: foreach, while, repeat, dowhile, if-else-then, label, goto, continue and break



## Command Scripts (con't)

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- Script\_Example

```
.CONTROL
```

```
    setplot tran3
```

```
    measure max_v1  max v(1)
```

```
    measure max_v2  max v(2)
```

```
    set numdgt = 12
```

```
    echo "The maximum value of v(1) is " $max_v1 > out.$$
```

```
    echo "The maximum value of v(2) is" $max_v2>>out.$$
```

```
    shell cat out.$$
```

```
    shell rm out.$
```

```
$
```

```
.ENDC
```



## Command Scripts (con't)

- These features allow the user to generate complex scripts to automate the simulation and analysis process
- SmartSpice also fully supports standard I/O redirection operators and backquote substitution which allows shell commands to be evaluated and the results to be assigned to internal SmartSpice variables
- This allows importing a results file and extracting more data without the time penalty of re-running the simulation



## Parameters and Options Unsupported in Berkeley's SPICE (con't)

- Option EXPERT
  - The option EXPERT is supported in both 3.0 and 3.1 models
  - This option can be used to detect, before and during simulation, possible problems in BSIM3 models such as:
    - negative conductances GM, GDS and GMBS
    - negative capacitances
    - active smoothing functions
    - positively biased bulk to drain or bulk to source diodes



## Useful .OPTIONS Statements

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- VZERO
  - Define the modified nodal analysis(MNA) formulation in SmartSpice .OPTIONS VZERO=2 is recommended when simulating large circuits
  - The option VZERO=2 is supported in both 3.0 and 3.1 models
  - This option is recommended when simulating in the time domain relatively large circuits with hundreds and thousands of transistors
  - It accelerates simulation and increases accuracy of simulation results
- RAWPTS
  - Used when a large amount of output data is expected. SmartSpice writes data into the output file every RAWPTS points, e.g. .OPTION RAWPTS=300 and can speed up the simulation due to the smaller memory footprint
- FORMAT
  - Provides a compact format for .MEASURE output results



## Useful .OPTIONS Statement (con't)

- POST
  - Automatically generate a rawfile without using the -r command line option. If the post option is used without a value, then a value of 1 is assumed. The name of the rawfile is derived from the name of the current input deck with a ".raw" extension.
  - The flag for the POST option:
    1. binary
    2. ascii
    3. single precision binary
    4. XDR binary
    5. XDR single precision
- Now SmartSpice automatically allows for binary ordering differences between platforms without user interaction



## Useful .OPTIONS Statement (con't)

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- ASPEC
  - If ASPEC option is specified, then the default value of the SCALE and SCALM is 1.0e-6, e.g.  
    .OPTIONS ASPEC
- POSTRAWPTS (PRPTS)
  - This option allows post-processing when using RAWPTS option .OPTION rawpts=300 prpts
- TMAX
  - Set the maximum internal time step e.g.  
    .OPTIONS TMAX=5N



## Optimizer

- The Optimizer is a general purpose optimizing engine that requires initial and target parameter values to be set. The optimizer then iterates these parameters until the target values are reached
- The optimizer provides a comprehensive interface and an interactive display system for visualizing the optimization process as it is executed
- There are no restrictions on the type of circuit analysis that can be performed. Circuits can be optimized in steady-state, frequency, and time domains



## Optimization Example

- This example shows how to use the optimizer to select the transistor widths of M1 and M2, so that the trip point can be set to 1.55V, with a maximum current through the inverter of 1.9mA
- The trip point and the maximum current values are known as the optimizer targets
- The widths of the transistors are known as the optimization parameters



## SmartSpice Interpreter

- Allows user-defined models to be quickly and simply added to SmartSpice using C language syntax
- Powerful interactive debugger facilitates development / verification of new models
- Allows new models to be compiled into dynamic libraries which execute very quickly
- Provides extensive interface functions to SmartSpice internal data structures and procedures
- Very suitable for collaborative model development between Simucad and its partners



## Productivity – Parallel SmartSpice

- Parallel architecture of SmartSpice allows design departments to maximize simulation throughout using floating parallel threads to utilize full capacity of computer networks
- 64 bit SmartSpice allows big jobs and output files to be processed in a timely manner (multi-million device circuits)



## Parallel SmartSpice

- Other Approaches to Speed Up Circuit Simulation?
  - Methods used in timing simulation:
    - Table Lookup Methods
    - Event-driven simulation
    - BOTH METHODS LEAD TO A LOSS OF SPICE ACCURACY
- Simucad's Approach: Parallel SmartSpice
  - Retains all spice advantages:
    - Arbitrary circuit geometries
    - Analog / Digital
    - Same accuracy in Simucad's implementation as SmartSpice
    - Multi processor capability to increase throughput



## Parallel SmartSpice: New Spice Performance Leader

- Supported platforms:

Sun	Solaris 8, 9-(32 and 64 bit)
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HP	HPUX 11.0
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Windows	2000/XP
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Linux	Red 7.3, 9.0, Enterprise V3-(32 bit and AMD-64)
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- Don't give up accuracy for speed!!



## Parallel SmartSpice: Circuit Simulation with SPICE in General

- Spice simulation for functionality, timing & power:
  - Arbitrary circuit geometries
  - Both analog and Digital
  - Accuracy
  - Lack of speed for large circuits
  - No chip level simulation if over 10k gates
  - Cut netlist into critical path for timing simulation



## Parallel SmartSpice: Circuit Simulation with SPICE in General

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## Parallel SmartSpice (con't)

- Parallel SmartSpice features state-of-the-art parallelization techniques:
  - Parallel model evaluation:
    - Automatic circuit/task partitioning
    - Automatic Job Scheduling and processor mapping
    - Blocking and Caching for limited interprocessor synchronization overhead
    - Support of BSIM3v3 (BSIM1, BSIM3v2)
  - Parallel Linear Solver:
    - Column-based task partitioning
    - Elimination tree-based level scheduling
    - Event-based Synchronization

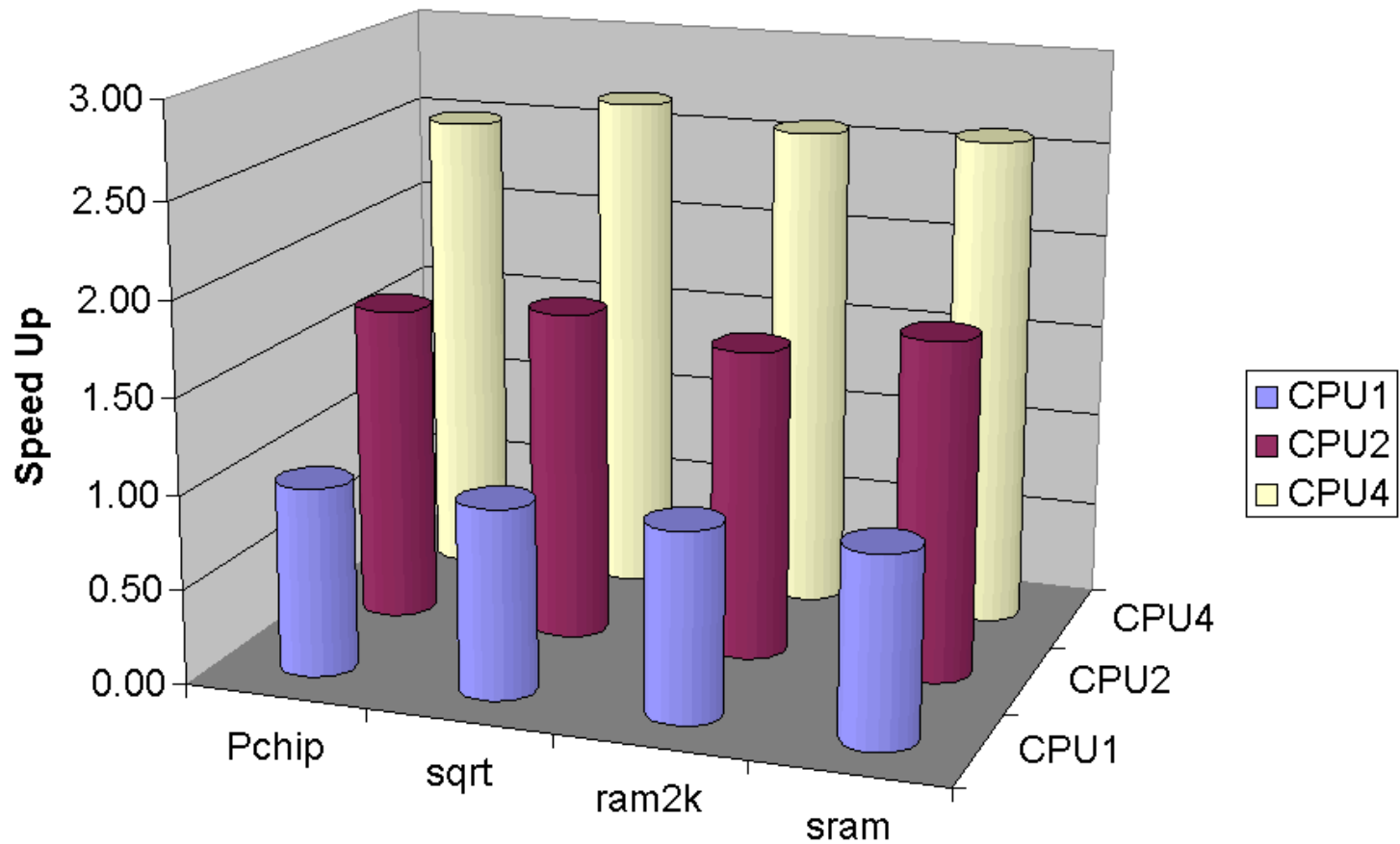


## Parallel SmartSpice (con't)

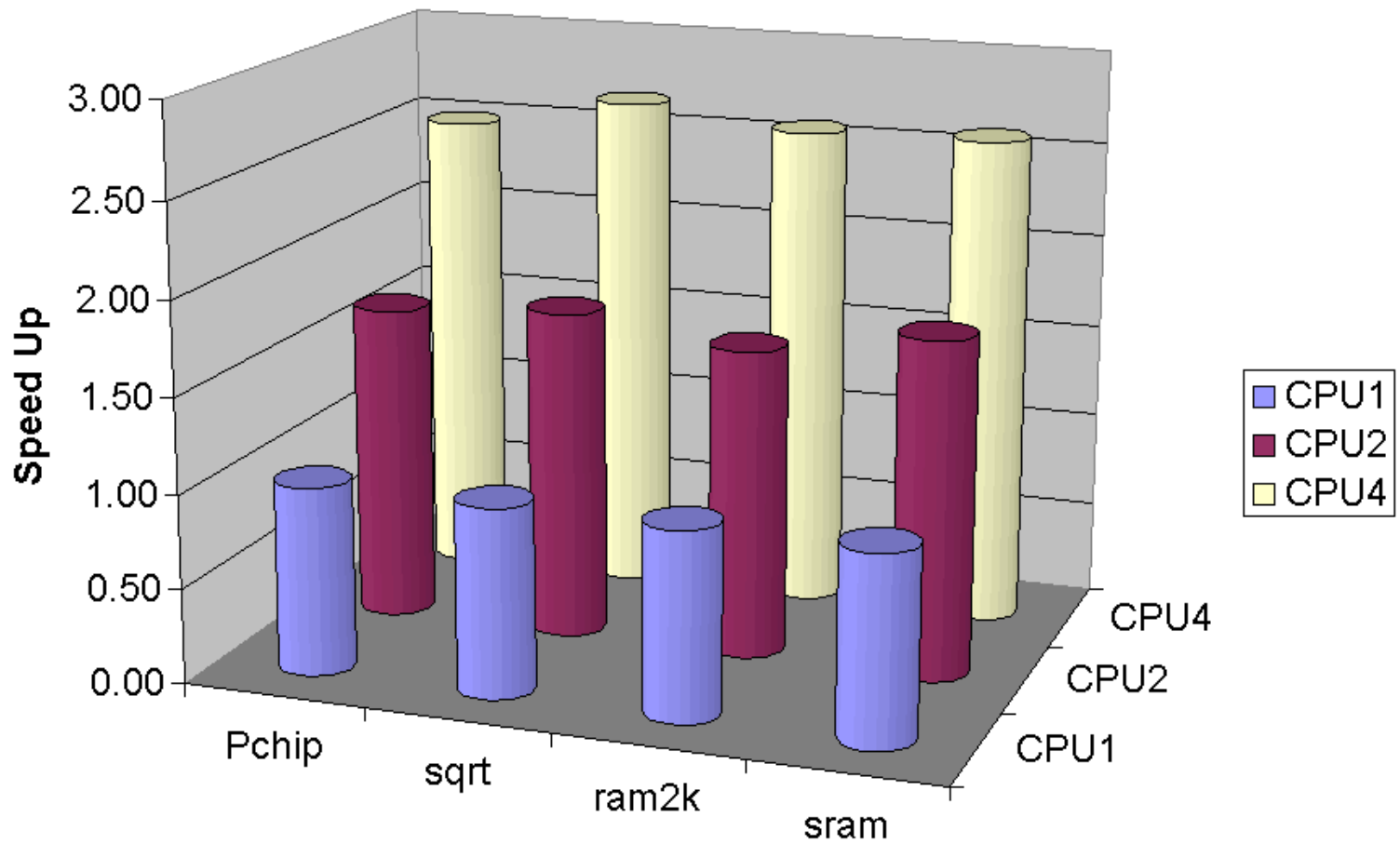
- Plus:
  - Speeds Up the simulation
  - Larger circuit sizes thanks to large amount of memory in parallel computers
  - No user partitioning required
  - The models remain virtually the same
  - No calibration required
  - No extra user intervention

*Only prerequisite: a Parallel Computer (shared memory desktop /desk-side)*

# Parallel SmartSpice - Linux



# Parallel SmartSpice - Windows





## Productivity – Better Designs: Speed, and Convergence

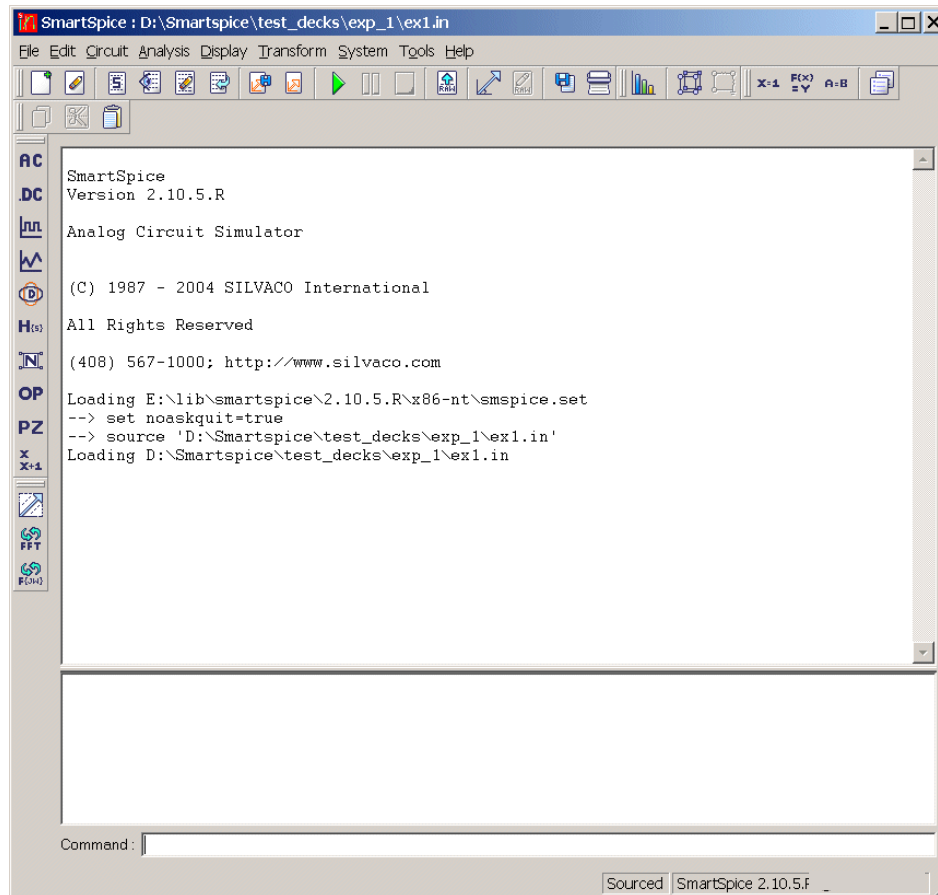
- Industry leading numerics implementation produces fastest simulation available
- Robust code provides first-pass convergence for complex designs
- Stop&Go feature allows input to be interactively modified without losing completed simulation tasks
- New “StopCont” function allows modification while the simulation is running or stopped and restarted from paused point in simulation run



## SmartView GUI and Graphical Post-Processor

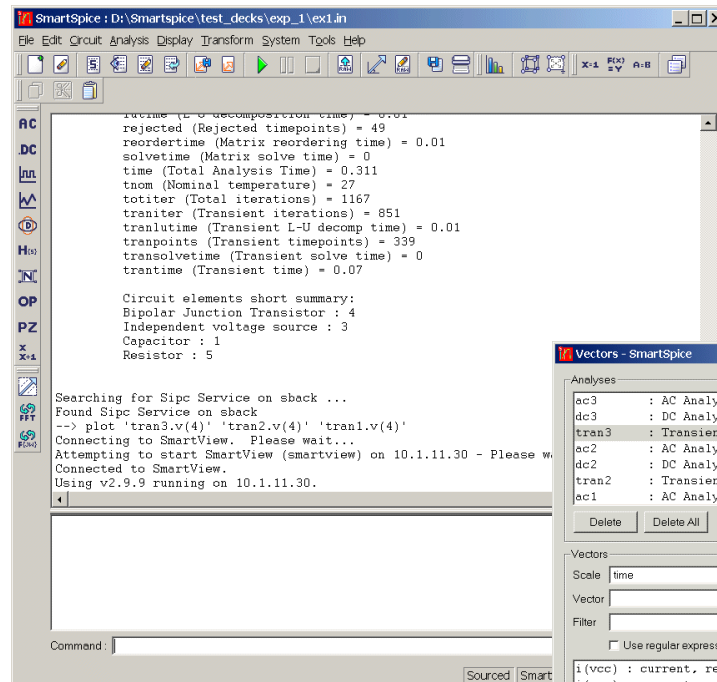
- Advanced and powerful features provided through convenient and user-friendly GUI
  - Supports visualization during interactive execution
  - Simulation data can be presented in many forms including; Smith Charts, polar plots, histograms and rectangular plots
  - SmartView enables easy tailoring of data presentation formats

# SmartSpice GUI

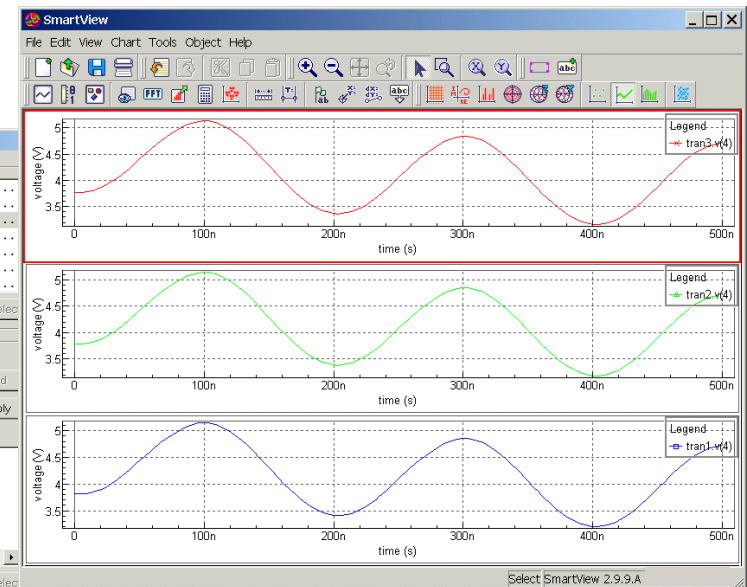
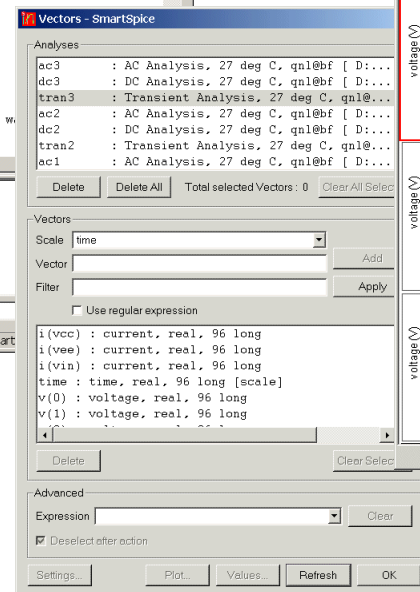


- New SmartSpice GUI introduces a cleaner and more productive interactive tool

# SmartSpice GUI (con't)



- Seamless hand off to graphical post-processor (SmartView)





## SmartView - Graphical Post-Processor

- Customizable multi-plot layout and viewing system
- Ability to change analysis type for selected vectors with a click of a button
- Calculator environment: Allows expression construction of SmartSpice built-in functions, macros and available vector from the rawfile
- Overlay feature capable of stacking new simulation results on top of previous results

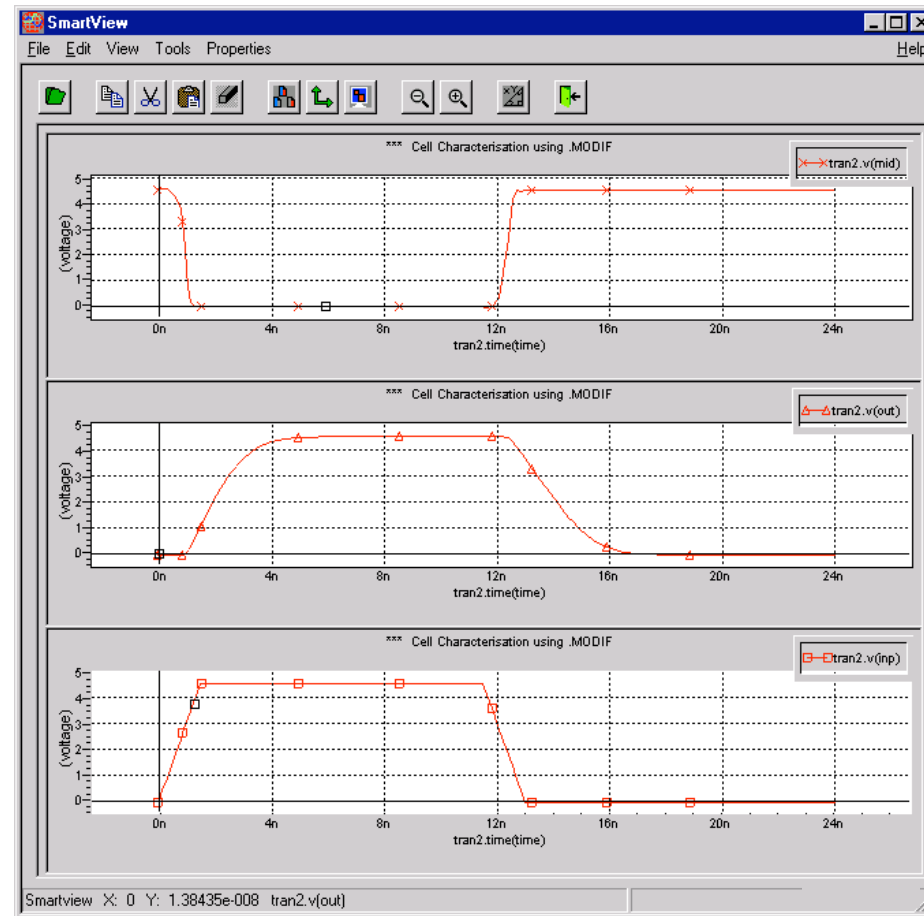


## SmartView - Graphical Post-Processor (con't)

- Expanded custom annotation for selected plots (for example: font size, switching units, colors, etc.)
- Ability to plot multiple vectors on a single plot with a secondary x and y axis
- Picture-in-picture in zoom mode

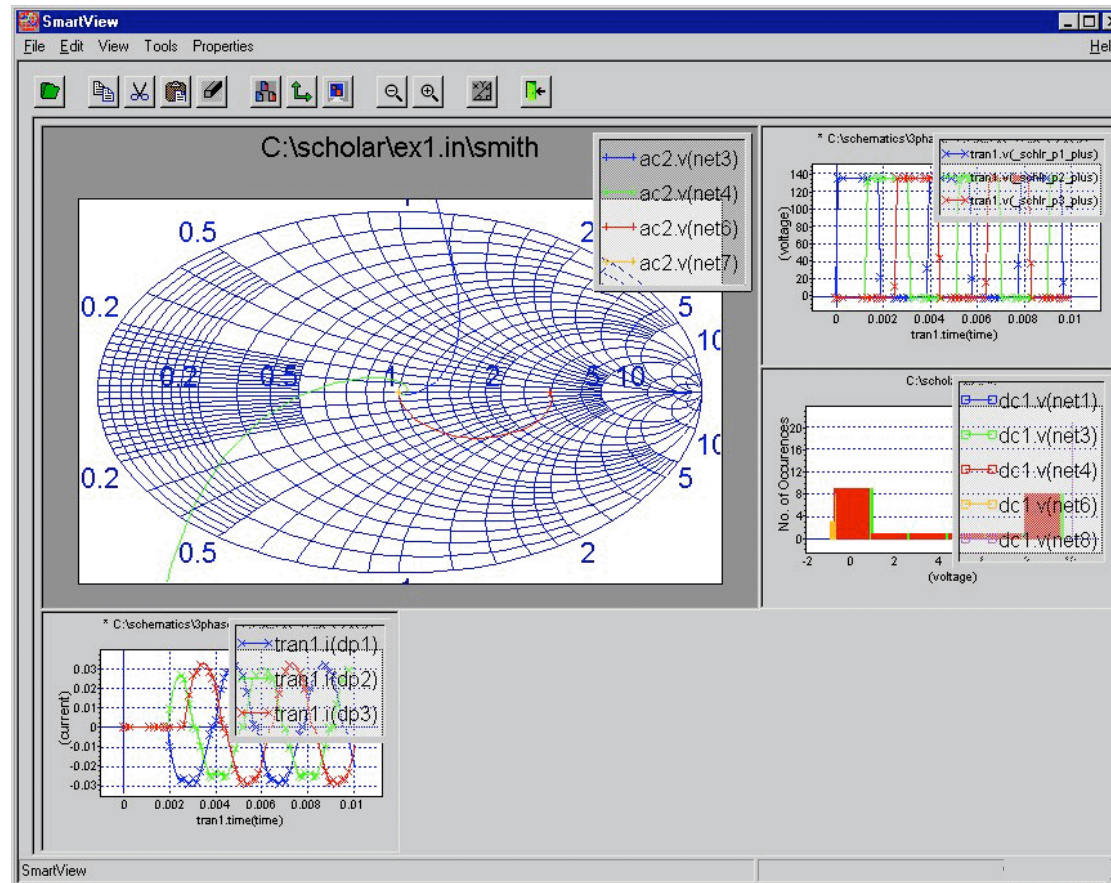


# SmartView - Graphical Post-Processor





# SmartView - Graphical Post-Processor





## HSpice™ and PSpice™ Compatibility

- SmartSpice uniquely offers compatibility with Hspice™ and PSpice™ that:
  - Preserves past investment
    - Designs completed using Hspice™ and Pspice™ can be re-simulated without modification
  - Reduces design inefficiencies and internal support requirements
    - Single fully-supported Spice vendor allows companies to focus on design



## HSpice™ and PSpice™ Compatibility (con't)

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- Creates new freedoms
  - Site licenses, enhanced models, superior features and analysis capabilities
- Makes Replacement Simple
- Simucad is the **ONLY** Spice vendor that offers and continually supports compatibility



## HSpice™ and PSpice™ Compatibility (con't)

- To summarize:
  - Backward compatibility is essential for smooth transition from existing Spice simulator to an improved Spice Solution
  - Preserves past investment
  - Provides new capabilities



## Integration with Leading CAD Vendors: Cadence - SmartSpice Integration

- The Cadence integration with SmartSpice allows easy use of SmartSpice in the Cadence design framework
- The integration uses the Cadence scripting system to enhance the tools provided so no further software is required
- The integration adds SmartSpice to the list of spice simulators available as the default option without disrupting the existing setup
- Results can then be displayed, in the waveform viewer as before
- Customer has the same Cadence operation with SmartSpice setting in the background



## Integration with Leading CAD Vendors

- Cadence - SmartSpice Integration
  - Tight coupling with Analog Artist 5.0, 5.033, 5.1.41 through OASIS interface
  - Includes Mixed-Signal simulation with VeriLog
  - Supports cross-probing and back annotation of simulation results
  - Seamless integration offering an additional more powerful SPICE engine without significant disturbance to the user environment and controls



## Platform Compatibility

- Identical Code available on both Windows 2000/XP , UNIX and Linux
- SmartSpice provides the ONLY available high performance Spice solution to meet the needs of analog designers as Linux emerges as a significant design platform
- Platform compatibility allows netlists to be simulated on either UNIX or PC platforms providing portability of designs across facilities or between home and work



## Advanced SPICE Model Implementations: SmartLib

- Dynamically linked library of SmartSpice device models
- Can be shared with all Simucad products, e.g. UTMOST, SPAYN, MixedMode, TCAD
- Easily maintained
  - Revisions to the model code can be downloaded by the user from the web, without the need to request new versions of the product from Simucad
  - One set of code for all products
  - Model updates are quick to implement and get to the user



## Supported Platforms



- Workstation
  - SUN            Solaris2 5.8 and higher
- PC (Intel Pentium, AMD Athelton and later)
  - Windows      2000 XP
  - DOS
  - LINUX         Redhat 9.0, Enterprise 3.0



## Supported Platforms

- Identical Code available on both Windows 2000/XP, RedHat Linux and UNIX
- SmartSpice provides the ONLY available high performance SPICE solution to meet the needs of analog designers as Linux emerges as a significant design platform
- Platform compatibility allows netlists to be simulated on either Unix, Linux or PC platforms providing portability of designs across facilities or between home and work
- Built-in capabilities to allow for binary differences between platforms



## Problem Diagnostics

- The SmartSpice diagnostics help the designer to rectify a problem in a timely manner
- SmartSpice offers very powerful internal diagnostics based on the EXPERT option. The diagnostic information assists designers with any convergence problems that occur during simulation
- The EXPERT option detects:
  1. Possible problems in the netlist, e.g. nonconvergent nodes and devices
  2. Nonphysical and unrealistic device and model parameter values.
  3. Discontinuities in the model equations.
  4. Unrealistic bias conditions during simulation.



## Searching a Model Library

- It is not possible to cover wide ranges of device sizes with a single model
- Search model library based on the width and length of the MOSFET (Binning)
- Parameters WMIN and WMAX, LMIN and LMAX set the range for the model selection based on the device width and length
- A continuous model approach to get a greater model flexibility. This allows the simplicity of a single model approach with greater accuracy than the binning method



## Batch Mode Operation

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- Source input deck.
- Parse devices, models and statements
  - Warnings will be printed if parameters/options are not understood, expressions are invalid, etc.
- Execute analysis statements or execute commands in a `.CONTROL ... .ENDC` block
- Execute post-processor statements, e.g. `.SAVE`, `.PRINT`, `.LET`, `.MEASURE`, `.GRAPH`, `.PROBE`.
- Save data in a rawfile, if required.
  - Using `-r` command-line option, or post deck option



## Generate Rawfile

- If the `-r rawfile` command-line option is specified, then all vectors mentioned in post-processor statements will be saved in the rawfile, e.g.

```
% smartspice -b filename.in -r filename.raw
```

- If `POST` option is used, then the rawfile will be generated automatically, e.g.

```
% smartspice -b filename.in
```

would generate the rawfile "filename.raw", if post is specified



## SPICE Modeling Services

- Modeling Service provides cost effective, fast turnaround and high quality models and is an alternative for many companies
- Suitable for new model evaluation
- Services Include:
  - Extraction of DC, AC (s-parameters), Capacitance, Temperature, Noise and SPICE parameters
  - Packaged parts or wafers are acceptable
  - Temperature range from  $-55^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$
  - All commercially available SPICE models supported
  - Model validation in accordance with Foundry Users Network (FUN) specifications
  - Worst case and corner model generation based on SPAYN



## Productivity

- New Level of Productivity for Design Departments and Designers
  - No more waiting for a few expensive server licenses
  - Simucad's Site Licensing Policy is designed to make it affordable to provide a license for every engineer
  - Speed, accuracy, convergence and technology coverage capabilities of SmartSpice take away limitations other simulation packages impose on designers



## Productivity – More Licensing: Site Licensing

- Simucad offers an affordable site licensing solution that enables companies to provide a SPICE copy to ALL designers
- Eliminates the problem of lost productivity caused by engineers waiting for a license to become available
- Compatibility with major simulators allows easy transition to a single SPICE vendor environment
- A user friendly licensing manager interface to help simplify administration



## Conclusion

- SmartSpice is a proven spice simulator with a large customer base and founded on years of experience extracting device models
- Compatibility with other spice simulators offers fast and efficient upgrade to more extensive model set
- SmartSpice is evolving all the time to keep pace with it's customer requests for greater capability to deal with state of the art circuit development and processes
- With VPN and FlexLM licensing options the power and flexibility is unmatched in the industry