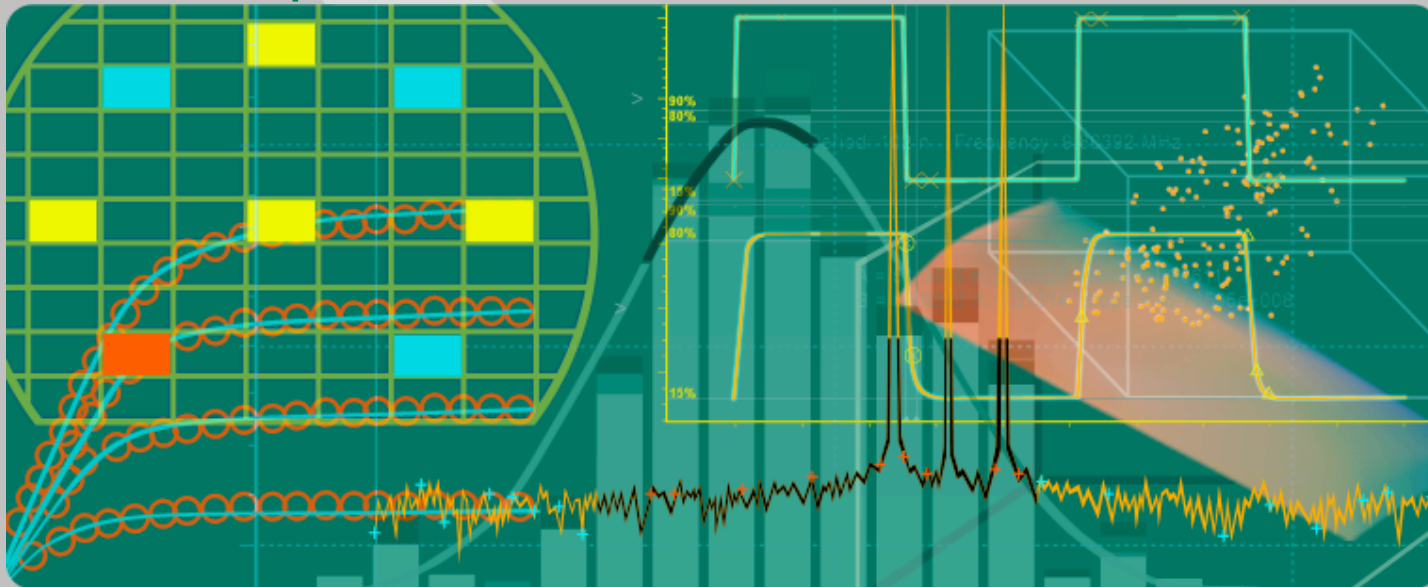
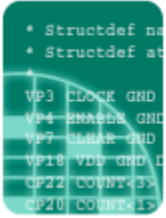


SmartSpice Analog Circuit Simulator Product Update

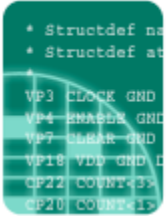


Summer 2004 Update



Agenda

- SmartSpice Products
- SmartSpice General Features
- SmartSpice New GUI
- SmartSpice New features
- Supported Models and Modeling services
- SmartSpice Future Development Plans



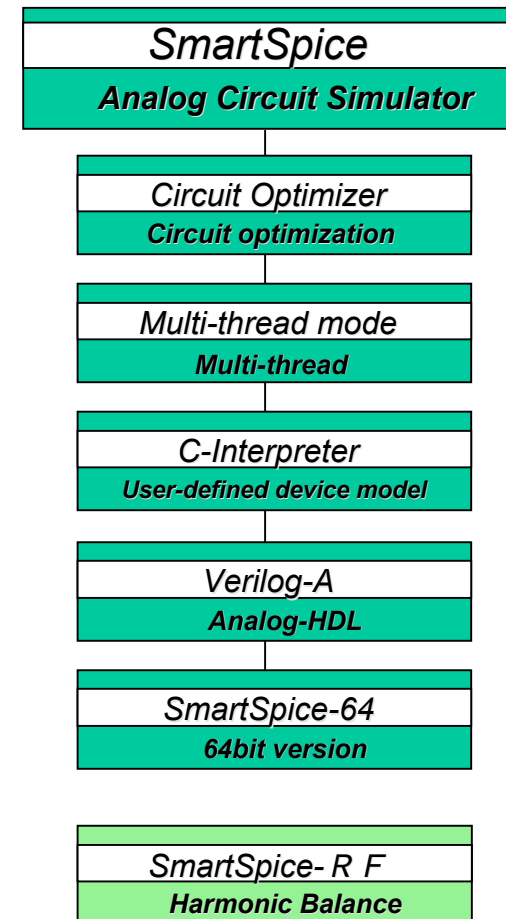
SmartSpice – Option Modules and Associated Products

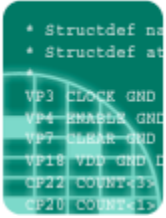
■ SmartSpice and its Option Modules

- **SmartSpice:** Analog circuit simulator
- **Circuit Optimizer:** Circuit optimization
- **Multi-thread mode:** parallel thread
- **C-Interpreter:** User-defined model
- **Verilog-A:** Language for analog behavioral modeling
- **SmartSpice-64:** SmartSpice 64 bit server version

■ SmartSpice Related Products

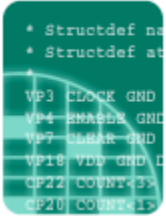
- **SpiceView:** Waveform viewer
- **Gateway:** Schematic editor
- **SmartSpice-RF:** Harmonic Balance-based simulator





SmartSpice - General Features

- 100% HSPICE™ compatible for netlists, models, analyses, and results => Current design environment can easily and simply be replaced by SmartSpice
- Provides the most accurate circuit simulation results for critical analog designs
- Largest capacity of any true SPICE circuit simulator
 - Robust solvers and device models can handle larger circuits with superior convergence - 400k active devices in 32-bit and 8M active devices in 64 bit version
 - Fastest run-time of any true SPICE circuit simulator
 - Simulation time at 2 to 4 times faster than other circuit simulators
 - Multi-thread option license for parallel operation
- Multiple solvers and stepping algorithms for robust convergence

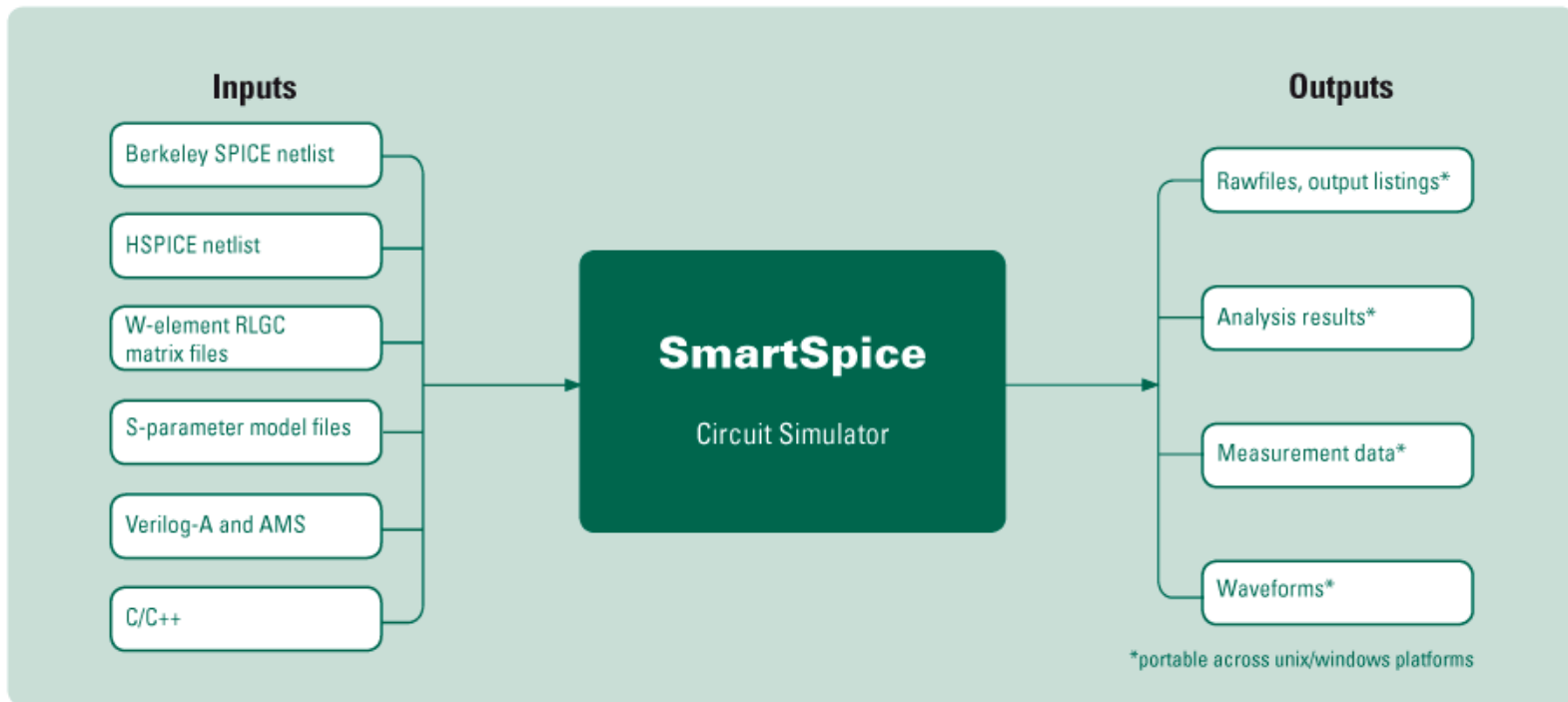


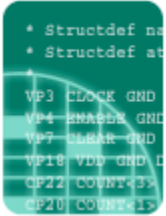
SmartSpice – General Features

- Largest collection of calibrated SPICE models for traditional technologies(Bipolar, CMOS) and emerging technologies(TFT, SOI, HBT, FRAM)
- Provides open model development environment and extensive behavioral capability with Verilog-A option
- Offers a novel transient non-Monte Carlo method to simulate the transient noise in nonlinear dynamic circuits

```
* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND D
CP22 COUNT433
CP20 COUNT417
```

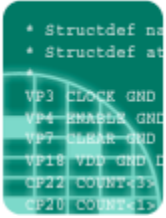
SmartSpice – Input and Outputs





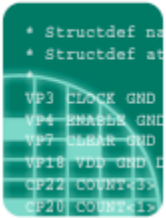
SmartSpice - New Graphical Environment

- Look-and-feel common to Silvaco products
- Supports completely identical GUI, multi-platform (UNIX/Linux/Windows) and designs (Gateway schematic files, SmartSpice results, etc) can be shared on different platforms
- Shortcut icon bar and other dialogs can be placed on/off main window
- Customizable shortcut icons and user's defined keyboard shortcuts
- Introduces a new inter-communication server that enables fast data transfer and seamless communication between products

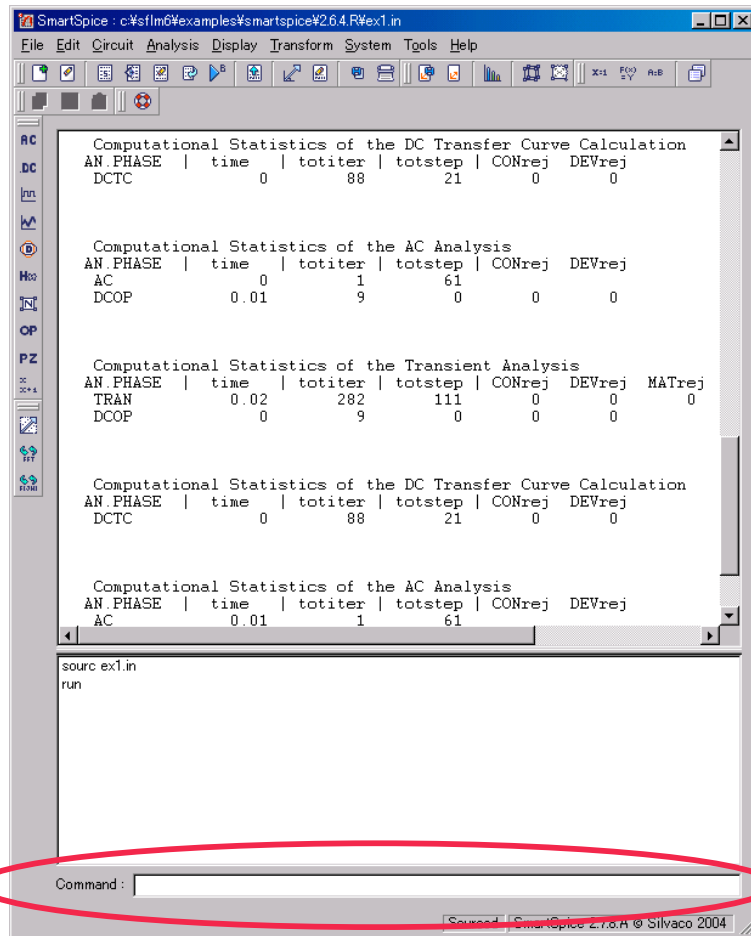


SmartSpice – SmartSpice New GUI

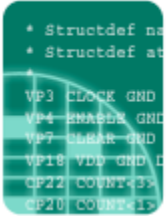
- Based on previous Windows front-end GUI
- Supports three types of simulation modes as before: Interactive window, batch, command line modes
- Seamlessly linked with SmartView - SmartSpice can transfer vector data directly to SmartView and control it for waveform plot creation
- Interactive simulation environment merged into one analysis dialog window
- Run time control menu for STOP/CONTINUE features (Stop/Continue/Pause a simulation job on the fly)
- New external text editor to create or edit an input deck



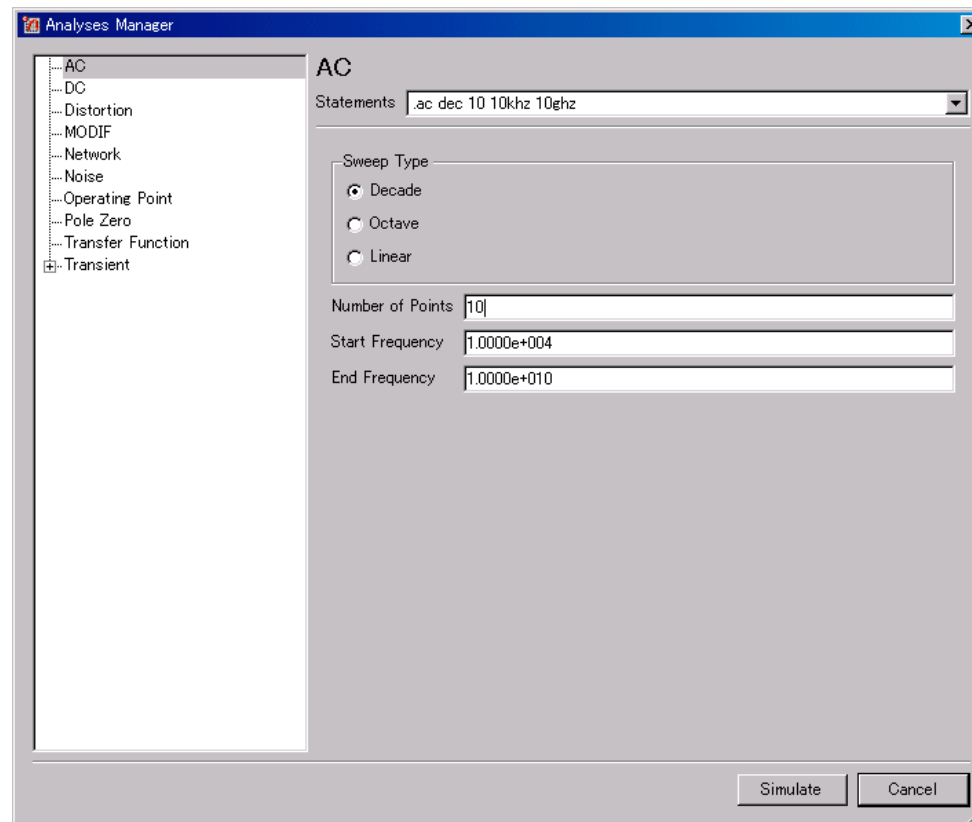
SmartSpice – SmartSpice New GUI



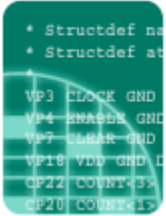
- Interactive operation environment with editable shortcut icons
- Intuitive GUI to control various kinds of SmartSpice operations completely common to different platforms
- Command line interface embedded in SmartSpice main window for keyboard operations



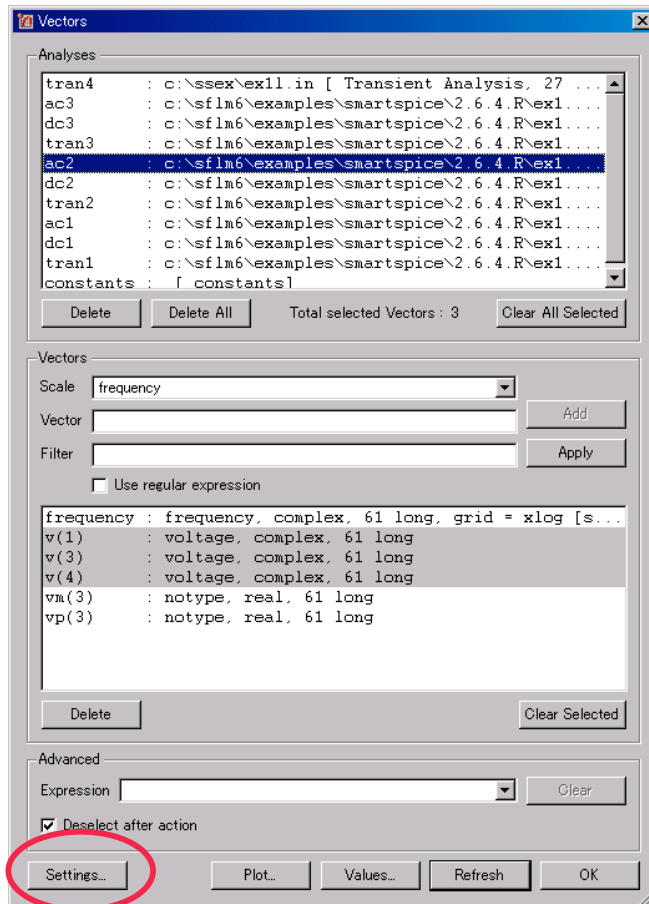
SmartSpice – Interactive Analysis Dialog



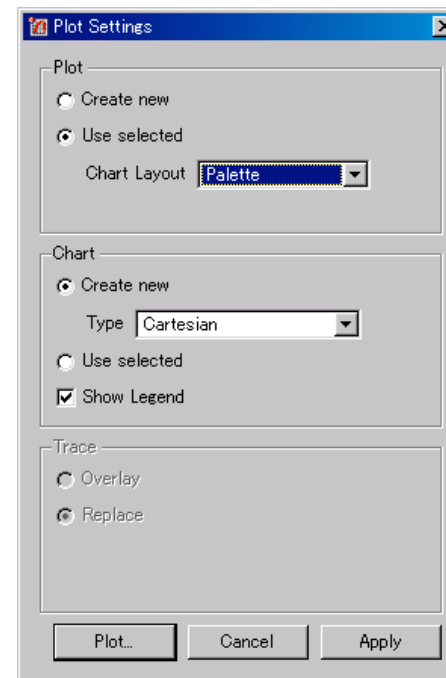
Interactive analysis dialog.

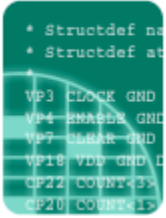


SmartSpice – Seamless Link with SmartView



- Vector selection and setting menu dialogs for plotting waveforms and controlling SmartView





SmartView – Key and New Features

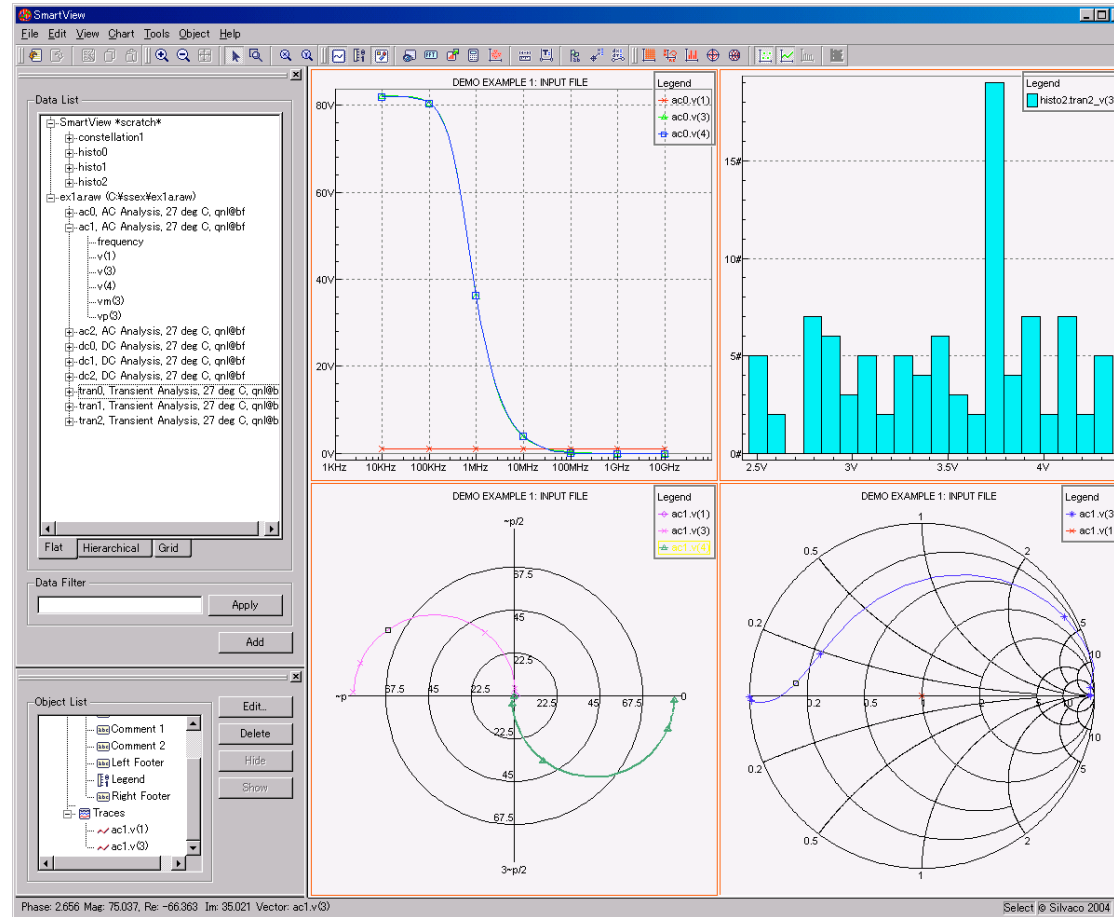
- New SmartView introduces a new graphical library set
- Seamlessly linked with SmartSpice/SmartSpice-RF, and Gateway -- can also be used as a stand-alone viewer
- Intuitive drag and drop operations, customizable shortcut icons, and keyboard shortcuts
- Multi-layout view and waveform splitting and merging feature
- Smith, Polar, and spectral plots suitable for RF applications
- Marching Waveforms - real time waveform plotting via SmartSpice and Gateway
- Various kinds of post-processing features, such as Vector Calculator, FFT, Probe marker, and measurements

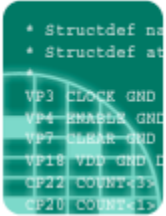
```

* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 BRAGG GND
VP7 CLEAR GND
VP18 VDD GND D
CP22 COUNT433
CP20 COUNT413

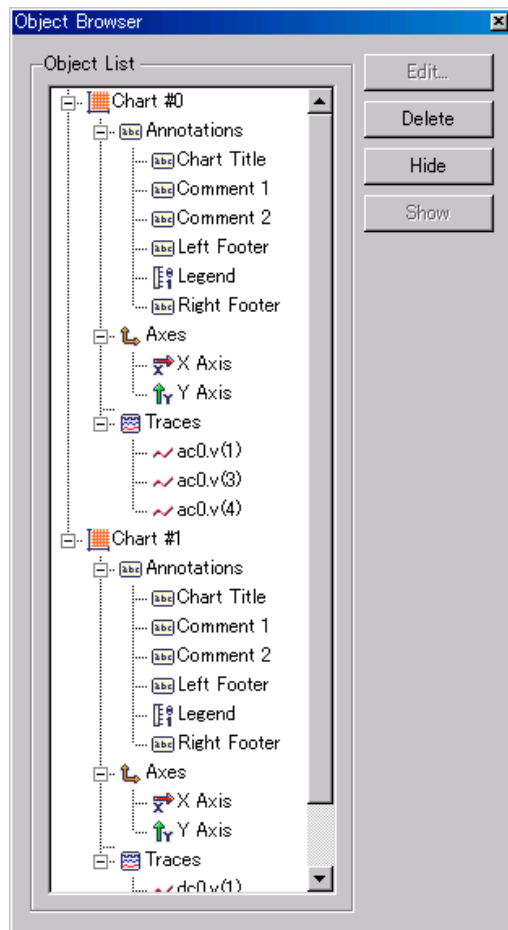
```

SmartView – Multi-Layout View

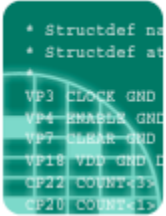




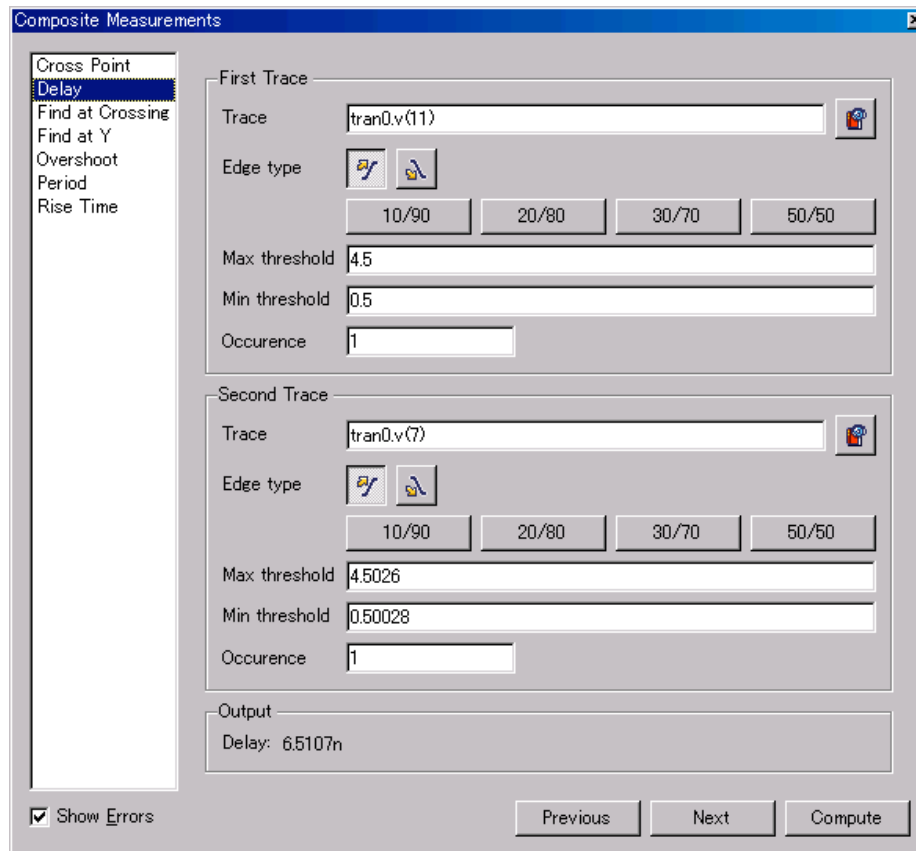
SmartView – Control Menu Dialog



- Three control dialogs can be docked with the main windows : Data Browser, Object Browser, and Trace Legend
- Data Browser is used for vector selection and chart creation.
- Object Browser and Trace Legend are available for managing all object attributes on created chart(s), and plotted vectors/legend



SmartView – Measurement Tool



Measurement environment in SmartView

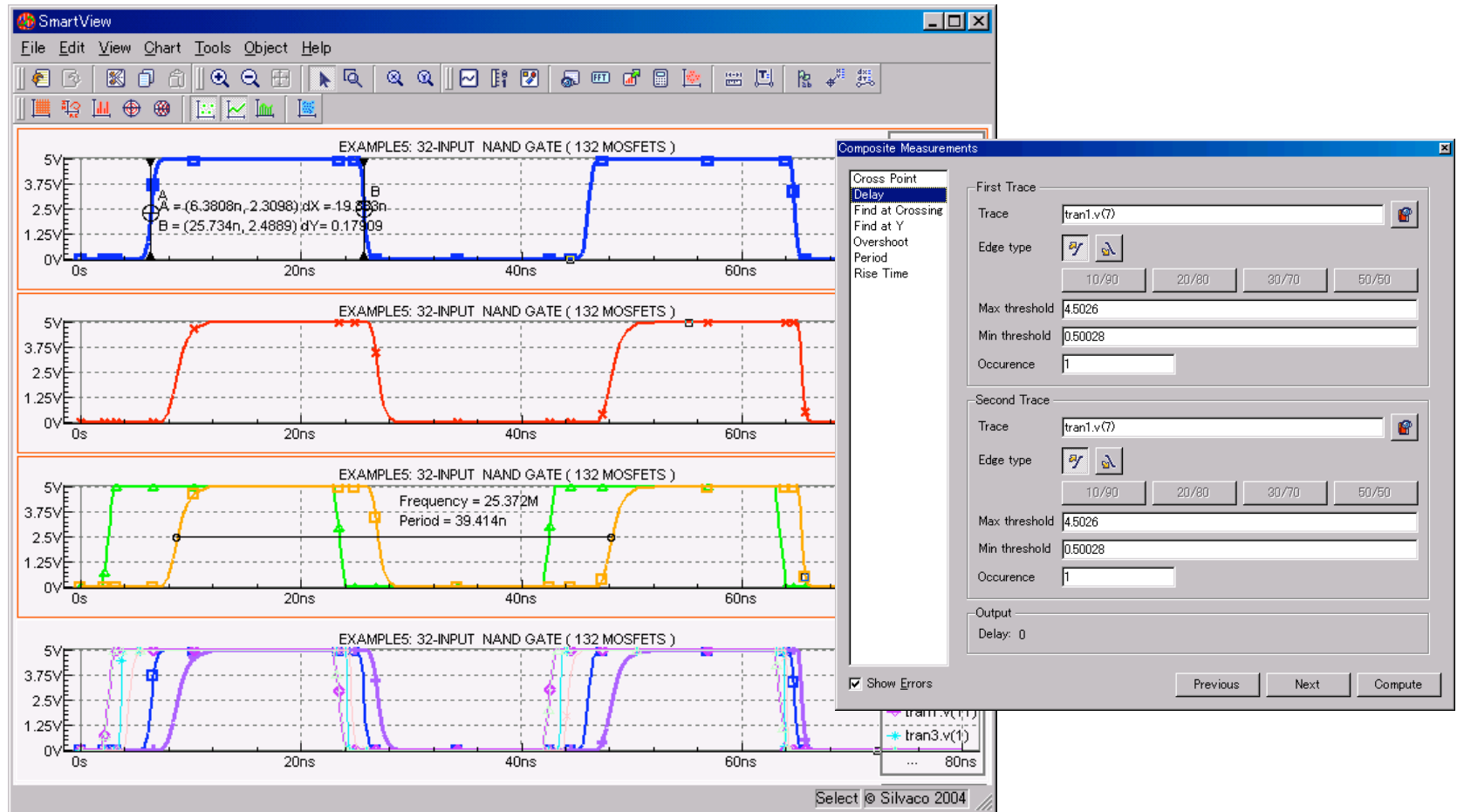
- MIN/MAX, AVG, Deriv, Delay, Rise/Fall time, etc (post-processor version of .measure statements)
- Probe marker, FFT, Eye Diagram, Vector Calculator, and so on

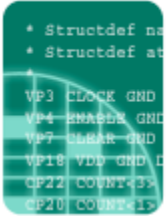
```

* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 BRAGG GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT433
CP20 COUNT413

```

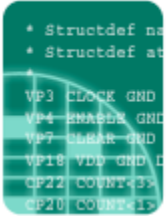
SmartView – Measurement Tool





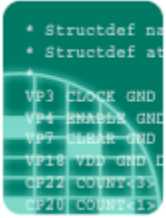
SmartSpice - New Features

- Stop/Continue feature
 - Provides a capability to stop, pause and continue(resume) a running job during a transient simulation
 - Post-processor and CPU can completely be released when a simulation job is stopped and users can monitor a circuit operation and/or check an intermediate results
 - User may give priority to one of simulation jobs by temporarily pausing other SmartSpice jobs and releasing CPUs for the prioritized job when he wants to complete the simulation as soon as possible
- Split of foreground and background operations
 - Enables a user to make use of post-processing features (SmartSpice GUI window operations) without stopping a simulation. The simulation job is running as a background process but GUI operations are available as foreground.
 - An exclusive CPU may also be assigned to this foreground process



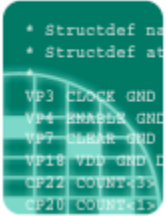
SmartSpice - New Features

- **New linear solvers**
 - Two more matrix solvers (suitable for a large circuit, for example, 100k active devices or more) has been added and now three direct and 2 iterative solvers are now supported.
- **Remote .alter(Unix only)**
 - Capability to distribute separated .alter jobs automatically onto multiple unix machines on network using unix remote shells.
- **Safe mode option**
 - New option to monitor system resources – disk space and memory usage during a simulation.
 - Pops up a warning window to avoid any possibility of losing a currently running job before system resources are exhausted

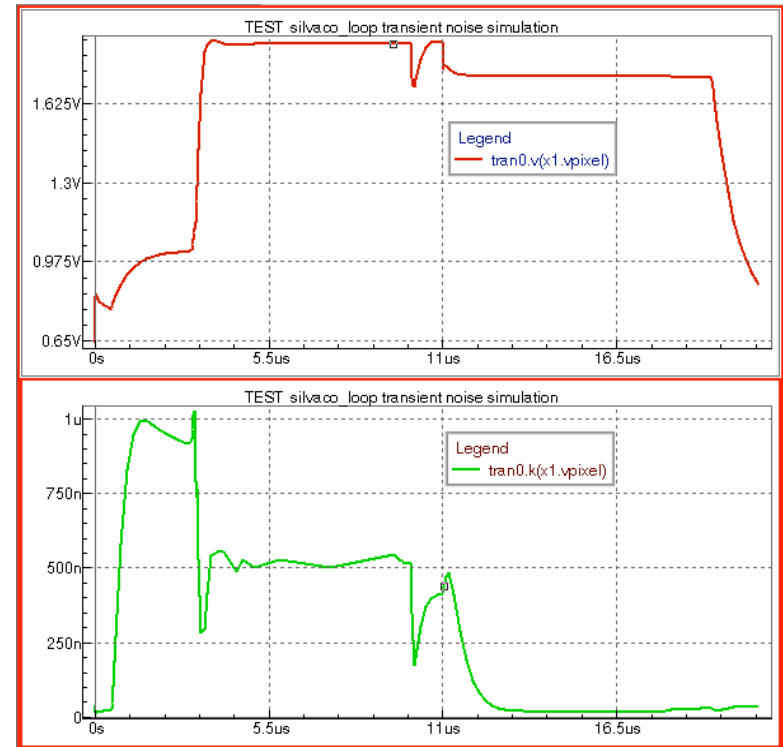
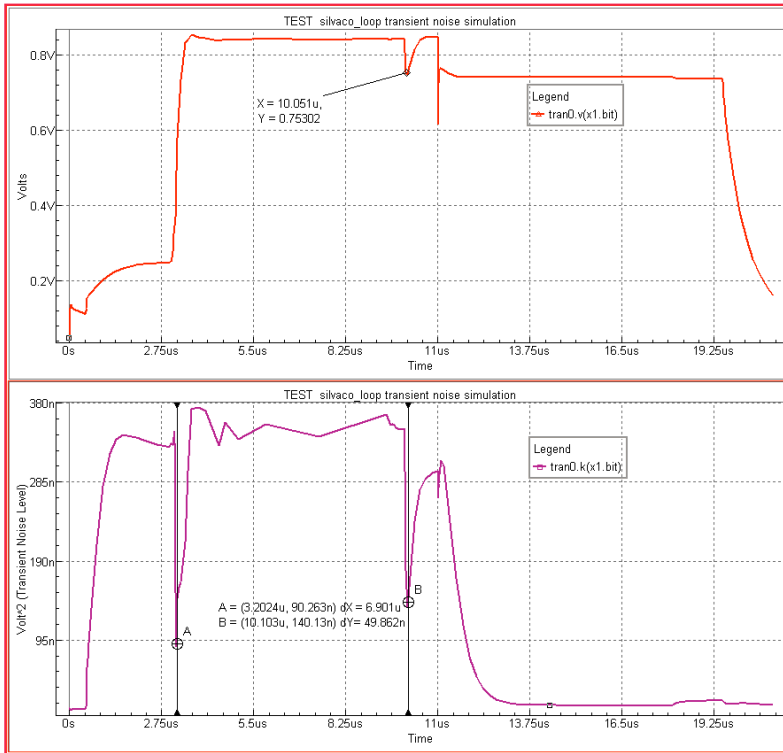


SmartSpice - New Features

- Transient noise analysis
 - Calculates total output noise(due to thermal, shot, and 1/f noises) at user's specified node(s) in a time domain simulation using non-Monte Carlo method
 - New noise source element (noise generator)
- Output noise control option
 - New control feature to turn on/off an arbitrary noise contribution component in which user is interested, i.e. thermal, shot, or flicker noise can be turned on/off for transient analysis.
 - New output variables of transfer function coefficient for (.noise)

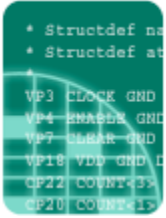


SmartSpice – Transient Noise Analyses



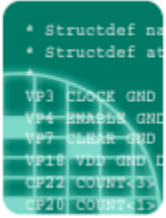
Transient noise simulation example:

Voltages(upper figures) and output noise(lower figures) waveforms observed at two different nodes during a transient simulation



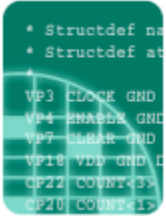
SmartSpice – New Features

- **.BIASCHK statement**
 - Extended measurement feature to monitor a voltage between specified element/device terminals, and detect if a breakdown can occur during a transient analysis
 - HSPICE™ compatible and SmartSpice's extended features
 - Can monitor internal and external nodes on various kinds of elements, devices, and subcircuits
- **.OVERSHOOT statement**
 - Checks all nodes in a circuit during a transient simulation and detect/report voltage spike
 - Reports node voltage exceeding Min/max voltage limit
- **.SHOW statement**
 - Outputs operating point info on specified device(s) during a transient simulation
 - Transient OP results are saved in a file at a specified time point or every specified time interval



SmartSpice – New Features

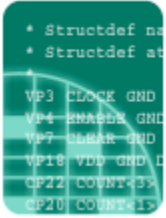
- **.EQUIV statement**
 - Provides aliases for model names in different library files
 - User can easily change different library files without modifying any descriptions on model names in device/element lines or in a library file
- **Multiple nest sweep feature**
 - Powerful parametric analysis feature for multiple variable sweep
 - Can be nested in more than two sweep loops
 - New option variable enables SmartSpice to load multi-swept raw data file and view waveforms much faster



SmartSpice – Device Models

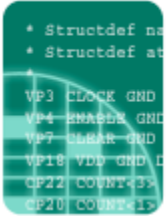
Devices models supported in SmartSpice/UTMOSTIII

- **Bipolar:** Gummel-Poon, VBIC1.2/1.1.5, MEXTRAM504/503, HICUM, Modella, UCSD HBT
- **MOS:** BSIM4/BSIM3v3.2.4, Philips MOS11, EKV, STARC/Hiroshima Univ. HiSIM1.2/1.1
BSIM3HV(Silvaco HV model)
- **TFT:** RPI poly-Si/amorphous-Si TFT models
Berkeley poly-Si model, Leroux amorphous-Si model
- **SOI:** Berkeley BSIMSOI(PD/FD), Florida Univ. SOI ver.7.5(PD/FD)
CEA/LETI, Philips MOS40
- **MESFET:** Curtice1/2, TOM-1/2/3, Parker-Skellern models
- **Other technologies:** Philips Juncap, Ramtron Ferroelectric Capacitance, VCSEL models



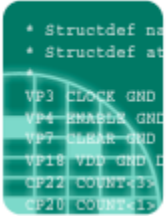
SmartSpice – Device Model

- SPICE modeling software and services
 - All device models supported in SmartSpice can be modeled by using UTMOSTIII
 - Silvaco can also provide high quality and cost-effective modeling services
- All supported models will be provided as SmartLib on Silvaco website



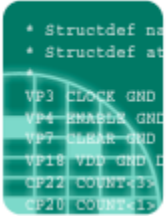
Modeling Service - Overview

- Silvaco has been providing SPICE Modeling Service for 20 years (since 1984) and many companies have made use of our modeling services
- Modeling Service is provided by using industry de-fact standard modeling software UTMOST III
- Silvaco is a leader in SPICE modeling, such as advanced device technologies, such as SOI, TFT, HBT, MESFET in addition to conventional CMOS and Bipolar technologies and also distributes associated circuit design tools
- Silvaco's TCAD and circuit simulator software enhanced the model validation from the device physics level to circuit simulation performance
- Silvaco generates vast majority of the discrete device libraries for the major companies



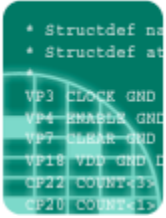
Modeling Service - Features

- Cost effective
- Fast turnaround services: typically two weeks for a CMOS process and one week for a couple of bipolar devices
- Provides a validated SPICE model with high accuracy
- **SmartSpice**, HSPICE, Spectre™, PSPICE™ compatible model generation
- Suitable for a new model evaluation
 - e.g. BSIM4, VBIC, Mextram, etc
 - More and more model parameters are nowadays used in a device model to take into account various kinds of device physics and that makes users too difficult to understand physical meanings of each model parameter.



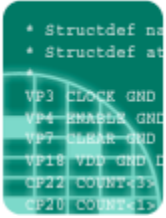
Modeling Service - Features

- Supports all major SPICE models
- Create a complete model for customer's specified target model
- Measurements on wafer or packaged parts provided by customer
- DC, AC (S-parameters), capacitances, temperature, noise measurements and modeling
- Wide range of temperature measurements covering -55°C to $+150^{\circ}\text{C}$
- Optional AC validation using a RO circuit
- Optional worst case corner model generation based on measurements with SPAYN, or skew data provided by customer



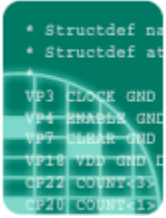
SmartLib – SmartSpice Device Model Library

- All model codes, such as BSIM3v3, Gummel Poon, etc. are currently integrated within one SmartSpice executable and are distributed to SmartSpice users as a package
 - The only problem is that it takes some time for Silvaco to deliver a SmartSpice package to users, even when developments for a model implementation into SmartSpice are already done. That's because we have to check full SmartSpice functionality before the shipment
- SmartLib is developed for avoiding functional dependency on SmartSpice versions and immediately releasing a new or updated model
- Once a new model development is complete, the SmartLib is provided as a library that can dynamically be linked with SmartSpice



SmartLib – SmartSpice Device Model Library

- Downloadable model libraries for SmartSpice
 - SmartLib supports all active device models implemented in SmartSpice
 - Users can immediately download SmartLib from Silvaco Web site when updated or released
 - SmartLib can easily be installed it onto a user's PC or EWS for an evaluation of a new technology model, or for an urgent problem(such as a bug fix in a certain model) when necessary
- Available for other Silvaco products which uses device models in SmartSpice in the future



SmartSpice – Future Development Plans

- Ability to express model parameter as a function of W/L and Area
- Release of SmartLib
- Development of a collection of special functions suitable for cell/core digital characterization
- Development of an open API a set of functions that will allow users to easily integrate SmartSpice into other applications
- BSIM5 model