

HIPEX Full-Chip Parasitic Extraction



Summer 2004 Status



SIMUCAD



What is HIPEX?

- HIPEX Full-Chip Parasitic Extraction products perform 3D-accurate and 2D-fast extraction of parasitic capacitors and resistors from hierarchical layouts into hierarchical transistor-level netlists using nanometer process technology
- These products are tightly integrated with the Expert Layout Editor for the complete design flow of DRC/LVS/LPE and RC parasitic extraction on one platform



Overview

- HIPEX Product Family Overview
- HIPEX-NET – Layout Device Extractor for HIPEX Products
- HIPEX-C – Capacitance Extractor
- HIPEX-RC – Resistance and Capacitance Extractor
- HIPEX-CRC – Network Reduction Tool



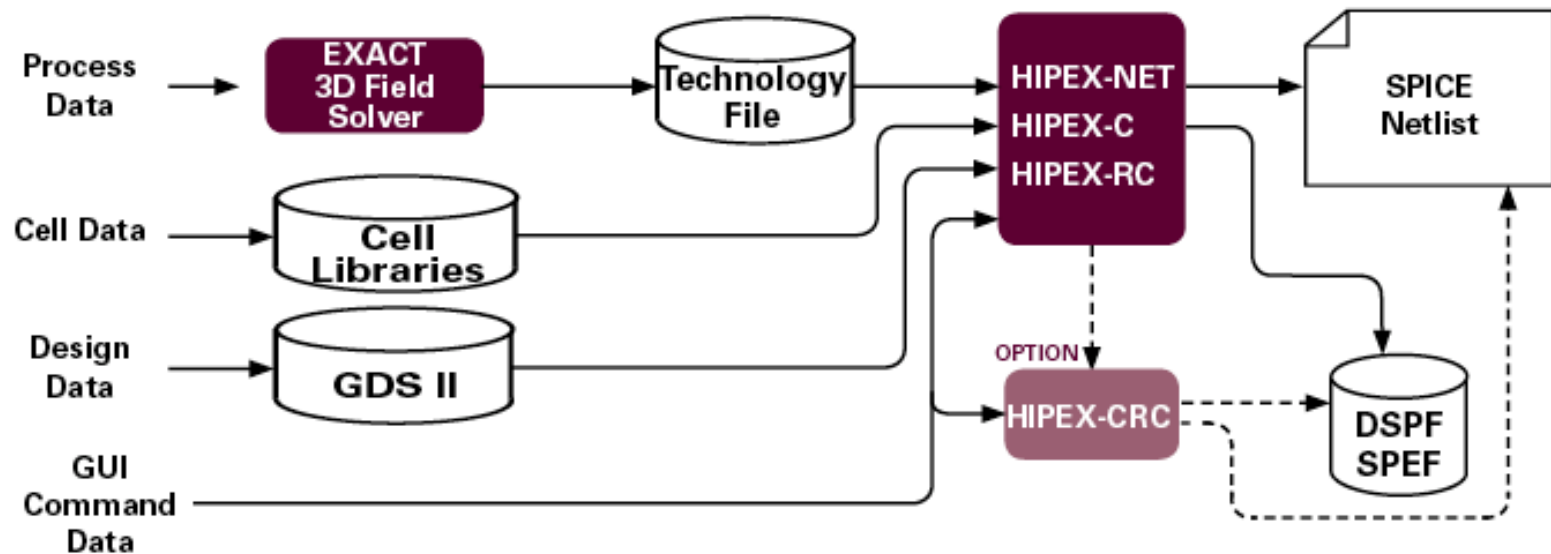
Overview

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HIPEX Full-Chip Parasitic Extractor: Product Design Flow





HIPEX Full-Chip Parasitic Extractor: Product Family Key Features

- Accurate and fast full-chip hierarchical extraction software
- Capacitance - extracts parasitic overlap, lateral, and fringe
- Resistance - extracts parasitics for lines, contacts, and vias; splitting long conducting tracks for accurate RC-distribution
- Selected net extraction for fast C and R extraction of critical path nets in SoCs and large memories
- Multiple parasitic extraction models to trade off between accuracy and run time efficiency
- Powerful scripting capabilities within technology files
- Output parasitic netlist files in SPICE, back-annotated schematic netlist, DSPF and SPEF formats
- Efficient network reduction for distributed parasitic RC networks
- Tightly integrated with Expert Layout Editor or used in stand alone operation



HIPEX-NET Device Extraction

- Integrated into Expert Layout Editor
- Supports Calibre™ and Dracula™ technology files
- Common Graphical User Interface for Solaris, Linux and Windows platforms
- Extracts hierarchical netlist preserving original layout hierarchy for easy analysis
- Extracts MOSFET, MESFET, BJT, JFET, diode, capacitor, resistor, and parameterized user-defined devices
- Performs electrical rule checking (ERC) for shorts, opens, dangles
- Accurate parameter extraction for non-45 and non-90 degrees devices
- Efficient memory usage for handling large designs



HIPEX-C Parasitic Capacitance Extraction

- Driven by user-defined technology file
- Back-annotates the schematic netlist with parasitic capacitors
- Striping algorithm and stripe database enables efficient parallelization for multi-processor machines
- Extracts parameterized user-defined capacitors using LISA scripting language to account for 3D effects
- Extracts parasitic coupling capacitors and diodes for full chip and selected nets
- Outputs SPICE capacitor netlists including detailed netlist with overlap, lateral, and fringe capacitance
- Offers different built-in capacitance models to trade off between accuracy and run time
- Uses in-built capacitance models and supports external capacitance rule files generated by EXACT for 3D accurate mode
- Extracts selected nets for fast parasitic C computation of critical paths



HIPEX-RC Resistance Extraction

- Driven by user-defined technology file
- Back-annotates the schematic netlist with parasitic resistors
- Extracts contact parasitic resistors
- Processes L, T, Cross and Bend resistor shapes
- Uses contact over-sizing and clustering to simplify resistor shapes
- Extracts netlist with parasitic resistors hierarchically for full chip or selected nodes
- Builds resistance database for merging into parasitic RC netlists
- Multiple extraction models and equation solvers are used for arbitrary shape resistors
- Splits long conducting tracks for more accurate RC distribution
- Provides output of selected nodes into GDS or CIF file for layout debugging purposes



HIPEX-RC Supports SPICE and DSPF

The screenshot displays the Hipex-RC software interface. The main window is titled "hipex_rc" and shows a text editor window with the following content:

```
hipex_rc
Version: hipex_rc 2.3.6.R (Mon Apr 05, 2004 9:00)
File Edit Bookmarks View Help
*|NET 50 0.000739PF
*
%|HIF
*
%|HIF *|I (16/26:2 I6 26:2 X 0.000000 47.45 10.45)
%|HIF *|I (15/20:2 I5 20:2 X 0.000000 34.85 29.25)
%|HIF
*
%|HIF *|S (50:7 34.85 29.25)
%|HIF *|S (50 43.75 15.00)
%|HIF *|S (50:9 48.40 15.80)
%|HIF *|S (50:1 34.85 16.80)
%|HIF *|S (50:6 35.10 16.47)
%|HIF
*
R400 50:7 50:1 2.490000
R401 50:6 50:1 0.023031
R402 50:6 50:2 0.032157
R403 50:5 50:2 0.035000
R404 50:6 50:3 0.032157
C413 50:7 VSS 0.000155002P
* x=35.7 y=16.65
C414 50 VSS 0.000142169P
* x=43.75 y=15
```

Below the text editor, a summary window displays the following information:

```
#resistors : 24
time(seconds): 0.00u 0.00
% current = 54
%summary data: net 54.
```

The status bar at the bottom indicates "Line: 1054 Col: 1 INS Dos RW" and "© Silvaco 2003".



HIPEX-CRC Network Reduction Tool

- Significantly reduces runtime of post-layout and post-route simulations
- Performs reduction by elimination of dangling RC elements, elimination of RC elements less than a user specified threshold, parallel/series merging and Scattering-Parameter-Based Macromodeling
- Performs networks reduction in linear time
- Handles RC networks with loops
- Preserve the same accuracy of simulation for reduced RC networks.
- Supports SPICE, DSPF, or SPEF formats
- Custom reduction algorithms using LISA Scripting Language for selecting subcircuits, cells, nets and thresholds



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HIPEX-Net Device Recognition

- Extracts
 - Field Effect Transistor (MOSFET, MESFET, JFET)
 - Bipolar Junction Transistor (BJT)
 - Diode
 - Passive device (capacitor, resistor)
 - Custom device (user-defined device)
 - Custom sub-circuit (user-defined device)
- Derived layers may be used for complex device extraction
- Accurate parameters extraction for 90 and 45 degrees geometry
- Specific model name can be defined for any kind of device
- Electrical and geometrical checks are performed
 - Bad shape (missing pins)
 - Bad connection (shorted pins)



MOSFET Transistor Extraction

- Pins extracted
 - Drain, Gate and Source pins are always extracted
 - Source and Drain may be on different layers
 - Substrate pin is optional
- Capacitor connected MOSFET are reported
- Parameters extracted:
 - Gate length and width are always extracted.
 - Compensation coefficient (WEFFECT) can be taken into account for bent gates
- Additional parameters are available:
 - Source area and perimeter
 - Drain area and perimeter



Bipolar Junction Transistor Extraction

- Pins extracted:
 - Collector, Base and Emitter pins are always extracted
 - Substrate pin is optional
- Diode connected BJT are reported
- Emitter area is computed and can be output in 3 different ways
 - By default HIPEX-Net outputs actual area in square microns
 - If Area Unit factor is set, a dimensionless result (Area Factor) is given using this formula: $\text{Area Factor}^* = \text{Emitter Area} / \text{Area Unit}$
 - User can also specify a fixed Area Factor value to be output for all devices

*Area Factor is computed the same way for MESFET and JFET devices and for diodes



JFET/MESFET Transistor Extraction

- Pins extracted
 - Drain, Gate and Source pins are always extracted
 - Source and Drain may be on different layers
 - Substrate pin is optional
- Parameters extracted
 - Length
 - Width
 - Area / Area Factor.
- The different ways to output Area Factor for BJT are also available



Diode Extraction

- Pins extracted
 - Plus and Minus
- Parameters extracted
 - PJ
 - Area / Area Factor
- The different ways to output Area Factor for BJT are also available
- Diodes extraction eventually enables a specific feature to compute Area Factor based on device width rather than area



Capacitor Extraction

- 2 Pins extracted
- Can extract a third pin for substrate
 - Name of the substrate node found for substrate pin is preceded by a \$
 - Written at the end of the capacitor statement
 - Allow a SPICE reader to ignore substrate pins for capacitors if needed.
- Computes geometry-based capacitance
 - Capacitor area and perimeter are extracted
 - Capacitance value is computed this way
 - $C = \text{AreaCap} * \text{AREA} + \text{PerimCap} * P$
 - Area and perimeter capacitance factors are defined in technology file
- Additional parameters are available
 - Length, width, area and perimeter.



Resistor Extraction

- 2 Pins extracted
- Can extract a third pin for substrate
 - Name of the substrate node found for substrate pin is preceded by a \$
 - Written at the end of the capacitor statement
 - Allow a SPICE reader to ignore substrate pins for capacitors
- Computes geometry-based resistance
 - Basic method: $R = \text{SheetResistivity} * L/W$
 - Accurate method: using head resistance, contact resistance, and outdiffusion correction parameters
 - 2D Field Solver for complex shape resistors
- HIPEX-NET also outputs L and W parameters for resistors



Custom Device Extraction

- Custom device allows extraction of any complex shaped device
- Up to 20 pins can be extracted for such devices from any layers
- The number of internal nodes can be provided for simulation needs
- SPICE statement reports
 - number of pins
 - number of internal nodes
 - pin lists



Custom Sub-circuits

- Custom subcircuit allow user to provide SPICE description of a complex device in a file
- Description file will be included to final SPICE netlist (thanks to .include statement)
- Up to 20 pins can be extracted for such devices from any layers
- Written in SPICE netlist like any standard sub-circuit instance call



Net Management

- Support LOCAL/GLOBAL or PORT text in layout
 - Priority order used is: global > local > port
- Electrical Rules Checking (ERC). HIPEX-Net checks and reports the following cases, dealing with hierarchy
 - Shorted nodes: two different nets are connected.
 - Can be renamed at user's request
 - Open nodes: several unconnected nets with a same name
 - Most frequent or alphabetically lower name is used
 - Dangle nodes: nets not connected to any device
- Back-Annotation
 - Use of schematic netlist to create layout vs. schematic map file
 - Output back-annotated flat or hierarchical netlist



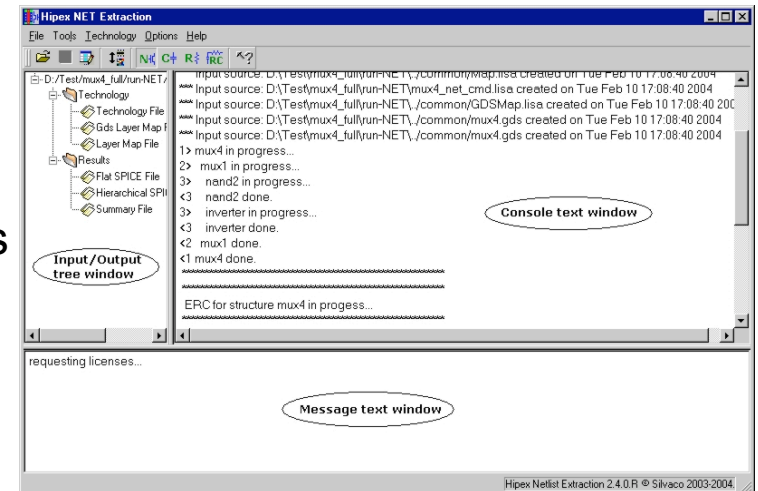
Hierarchical Extraction

- Automatic connectivity extraction for hierarchical layouts
 - HIPEX-Net automatically extracts hierarchical connections thanks to connection rules described in technology file.
- Supports use of Ports for hierarchical connection checking and extracting
 - Only hierarchical connections on ports are taken into account
 - Others are reported by a warning message
 - Port feature enables pins extraction for top cell
- Various options available for cell extraction
 - **IGNORE** - to prevent a cell extraction.
 - **FLATTEN** - to flatten a cell. Available for top cell.
 - **EXPLODE** - to bring cell components to upper level of hierarchy
 - **SMASH** - to flatten and explode a cell



HIPEX Technology File

- Describes rules for netlist extraction:
 - Local and hierarchical connectivity
 - Boolean operations for derived layers generation
 - Devices definition
- Supports Calibre™ and Dracula™ technology files
 - Converter scripts are available
- Technology files generated by easy-to-use Graphic User Interface
 - Integrated into Expert Layout Editor
 - Dedicated GUI also available for stand-alone use





HIPEX-NET Inputs and Outputs

Inputs

- Hierarchical layout (CIF or GDS)
- Rules and Option file (GUI)
- Schematic netlist (optional)

Outputs

- Flat or hierarchical SPICE netlist
- Back-annotated flat or hierarchical SPICE netlist
- Stripes Database for parasitic C extraction
- Summary file



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HIPEX-C – Capacitance Extractor

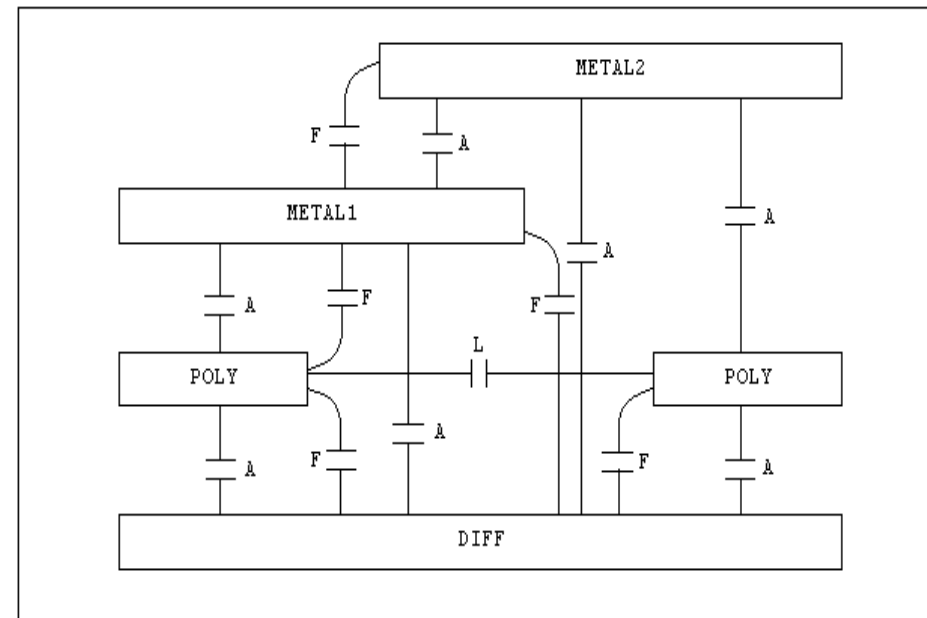
- HIPEX-RC – Resistance and Capacitance Extractor
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Parasitic Capacitor Recognition Patterns

HIPEX-C reports

- Coupling capacitors
 - Fringe capacitors (F)
 - Overlap capacitors (A)
 - Lateral capacitors (L)
- Ground capacitors
 - Fringe capacitors (F)
 - overlap capacitors (A)
- Parasitic diodes

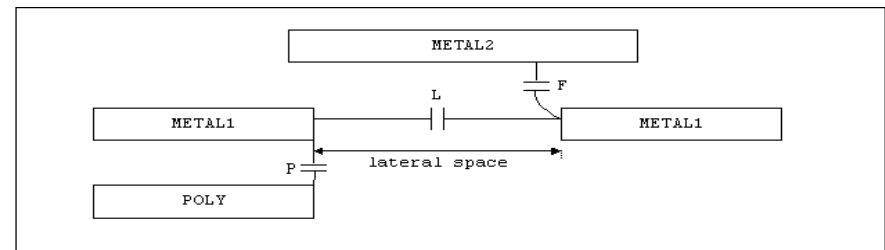




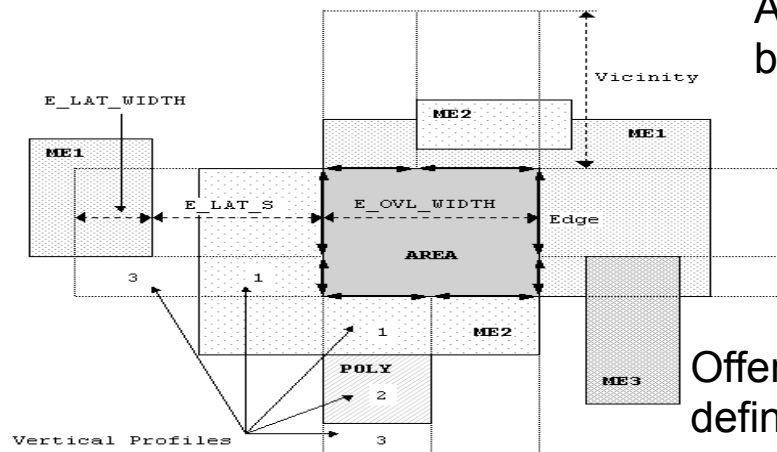
Multiple Accuracy Modes

3 accuracy modes to trade off between speed and accuracy

- BASIC mode allows fast first estimation
- MEDIUM and HIGH modes



Accounts for interrelation and shielding effects between layers



Offers accurate parameters extraction for user-defined or SPICE predefined models (more parameters for HIGH mode)



Selective Extraction

- Selective extraction allows to reduce the number of capacitors produced and focus on critical paths.
 - Cell based extraction
 - Node based extraction
 - Select critical nets
 - Ignore unwanted nets
 - Layer based extraction
 - Threshold
 - Coupling threshold permits to break coupling capacitors into ground ones
 - Ground threshold permits to ignore negligible ground capacitors



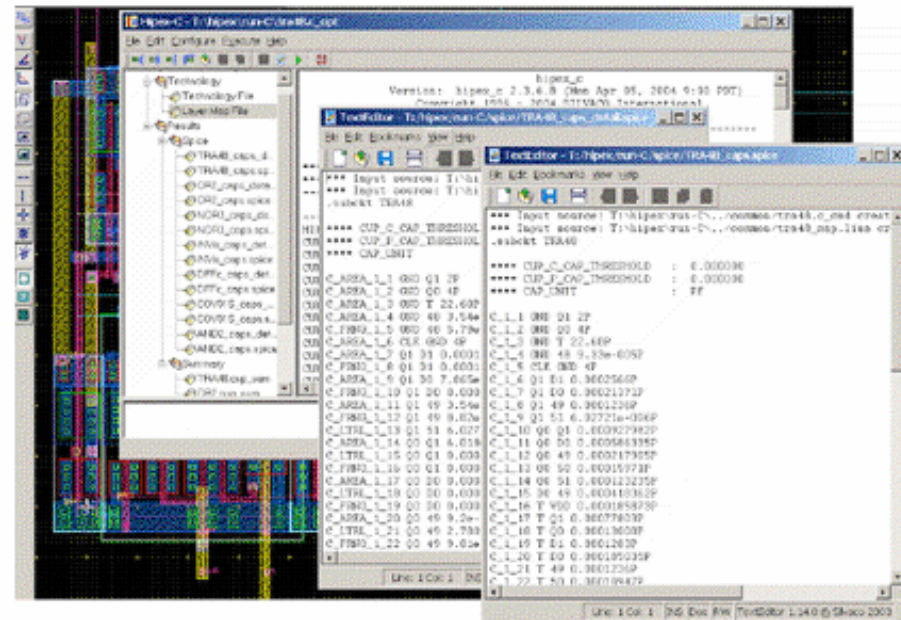
Technology and Capacitor Models

- Technology file defines layers interrelations and patterns required for extraction
- Supports external capacitance rule files generated by EXACT for 3D accurate mode
- In all 3 accuracy modes, HIPEX-C can call built-in capacitance models
- In HIGH and MEDIUM modes, HIPEX-C can call user-defined models to compute accurate capacitance
 - HIPEX-C extracts HIGH or MEDIUM capacitor parameters
 - LISA script user-defined procedure accesses to parameters extracted, and computes custom capacitor values
- In BASIC mode, HIPEX-C enables parameterized calls to predefined SPICE sub-circuits



HIPEX-C Outputs

- HIPEX-C outputs
 - Detailed list of capacitors per sub-circuit
 - Full C and devices SPICE netlist (flat or hierarchical)
- Optional outputs include
 - Backannotated netlists
 - Summary file
 - Capacitance Database (CDB) for RC extraction





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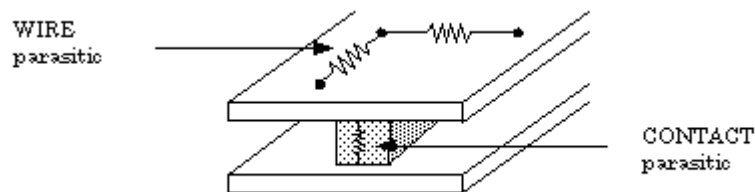
Parasitic Capacitor Extraction

- HIPEX-RC flow features the same abilities as HIPEX-C flow for capacitance extraction
 - Capacitor patterns (fringe, overlap and lateral) and diodes
 - 3 accuracy modes (BASIC, MEDIUM and HIGH) to
 - Speed-up extraction for huge layout (basic mode) or
 - Extract accurate parameters for user-defined or SPICE predefined models (HIGH mode) and
 - Account for shielding and interrelation effects (MEDIUM and HIGH modes)
 - Selective extraction
 - net and/or layer selection
 - cell selection

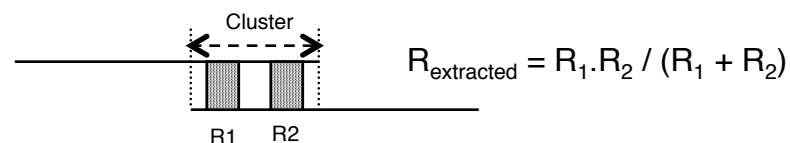


Parasitic Resistor Extraction

- HIPEX-RC processes wires and contacts/vias separately



- Contacts and vias give vertical resistors
 - Resistance depends on area resistivity factor given by technology
 - Clustering applies according to the wires they are connecting (parallel merge)

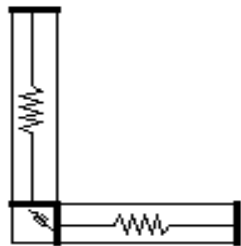


- Wires give horizontal resistors
 - They are fragmented into basic patterns before resistance computation
 - Sheet resistivity factor is used to compute resistance

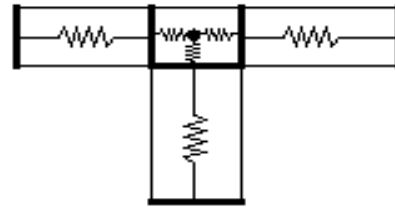


Parasitic Resistors Patterns

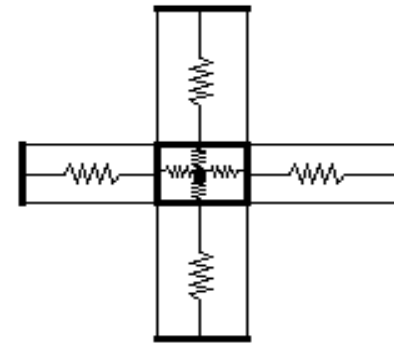
3 basic patterns are used to fragment wires



L-shape

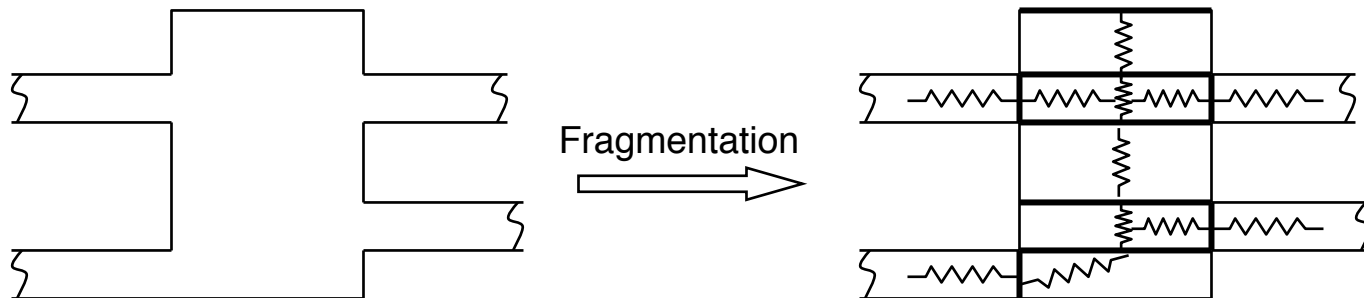


T-shape



Cross-shape

Complex shapes are split into several basic shapes for accurate extraction

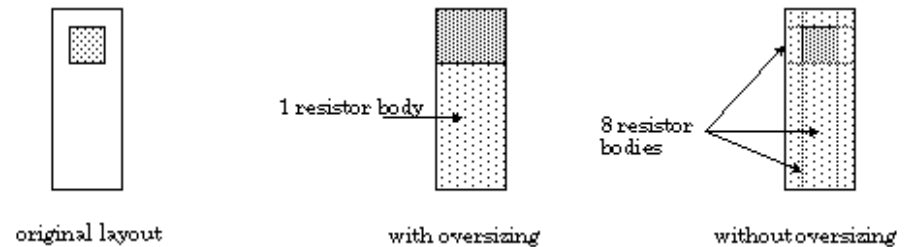




Fragmentation Features for Wires

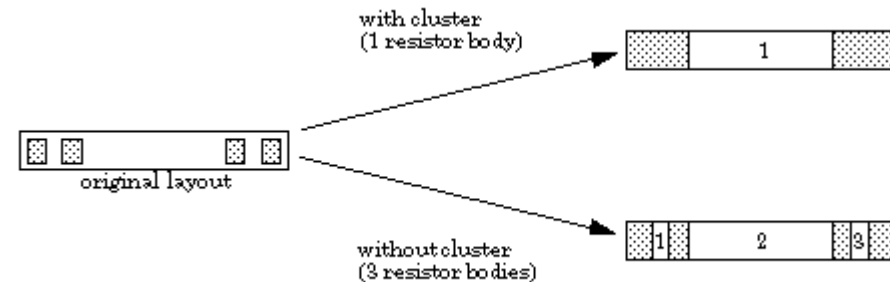
- **Oversize**

- Contacts are oversized to fit wires boundaries
- Doesn't affect contact resistance



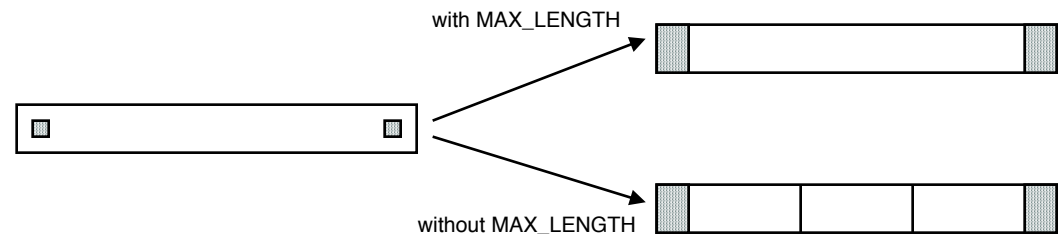
- **Cluster**

- Groups close contacts together to reduce number of resistors
- Contact resistance is updated (parallel merge)



- **Max length**

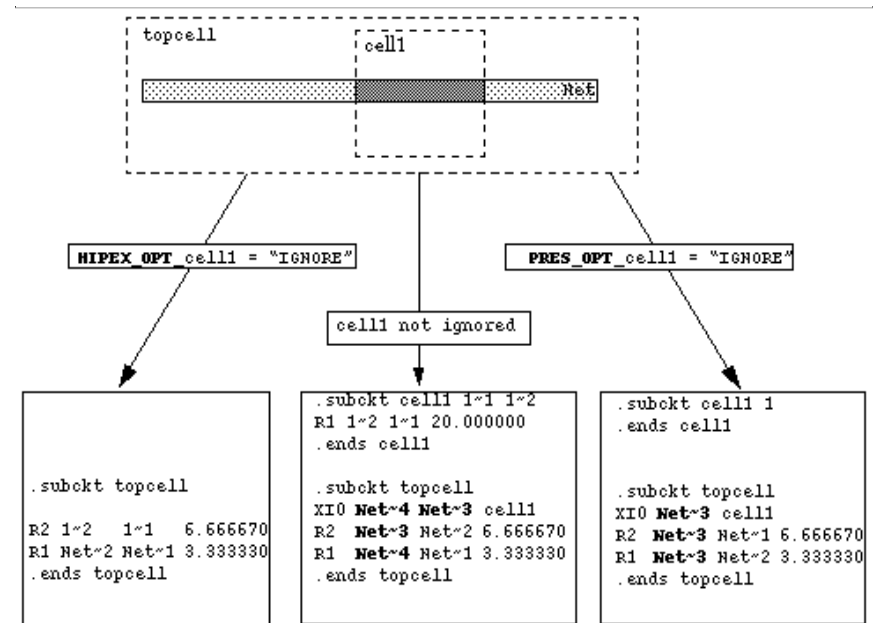
- Long wires are split
- Increases accuracy





Selective Extraction

- Selective extraction allows to reduce the number of resistors produced and focus on critical paths
- Various tools are provided
 - Threshold allows to discard any small resistor
 - Select/Ignore critical/unwanted nets
 - Select/Ignore layers
- Cell extraction is controlled by dedicated options
 - a sub-cell can be totally ignored or ignored only for parasitic extraction





Connectivity

- HIPEX-RC flow features the same abilities as HIPEX-NET flow for hierarchical or flat connectivity and net naming
- Sub-nodes are created for fragmented net
- Sub-nodes naming keeps entry point for simulation on named nets
- Pins are added automatically to sub-circuits to separate different connections on a same net

In this example nets “net1” from cell1 and “top_net1” from top cell will be fragmented. These nets are connected hierarchically in two different locations

```
.subckt cell1 net1
...
.end cell1

.subckt topcell
  XI1 cell1 top_net1
...
.end
```

Before RC extraction

```
.subckt cell1 net1~1 net1~2
  R1 net1~1 net1~2 0.253
  C1 net1~1 GND
  C2 net1~2 GND
...
.end cell1

.subckt topcell
  XI1 cell1 top_net1~12 top_net1~43
  R2 top_net1~12 top_net1~11
  R3 top_net1~43 top_net1~44
...
.end
```

After RC extraction:

- sub-nodes have been created
- pins have been added to cell1



HIPEX-RC Technology Files

- HIPEX-RC flow features the same abilities as HIPEX-NET and HIPEX-C for
 - devices and connectivity extraction (uses HIPEX-NET technology file)
 - capacitors extraction (uses HIPEX-C technology file)
- Technology file for resistors extraction
 - defines the resistive layers (contact/via or wires)
 - specifies resistivity factors
 - specifies geometry information for fragmentation features



HIPEX-RC Inputs and Outputs

- Inputs
 - Hierarchical layout (CIF or GDS)
 - Rules and Option files (GUI)
 - for device extraction (HIPEX-Net)
 - for R extraction (HIPEX-R)
 - for C extraction (HIPEX-C)
- Outputs
 - Full RC + Device netlist
 - Flat or hierarchical
 - DSPF and/or SPICE
 - Summary files

```
hipex_rc
Version: hipex_rc 2.3.6.R (Mon Apr 05, 2004 9:00)
net1
-----
*|NET 50 0.000739PF
*
%HIIF
*|I (16/26:2 16 26:2 X 0.000000 47.45 10.45)
%HIIF
*|I (15/20:2 15 20:2 X 0.000000 34.85 29.25)
%HIIF
*
%HIIF
*|S (50:7 34.85 29.25)
%HIIF
*|S (50 43.75 15.00)
%HIIF
*|S (50:9 48.40 15.80)
%HIIF
*|S (50:1 34.85 16.80)
%HIIF
*|S (50:6 35.10 16.47)
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C414 50 VSS 0.000142169P
* x=43.75 y=15
-----
#resistors : 24
time(seconds): 0.00u 0.00
-----
% current = 54
-----
%summary data: net 54.
```



Sample HIPEX-RC Extraction

- The graph on the following slide illustrates the influence of RC parasitic on a simple ring oscillator
- Extraction settings for HIPEX flows
 - Hierarchical layout made on a 0.12 micron technology
 - Use layout text for back-annotation
 - No threshold
 - No oversize or clustering for R extraction
 - BASIC mode for C extraction
- A very small layout
 - 80 mosfets, 740 R, 206 C (HIPEX-C flow), 2078 C (HIPEX-R flow)
 - Instant extraction
 - Simulated in less than 10 minutes by SmartSpice on a Linux machine



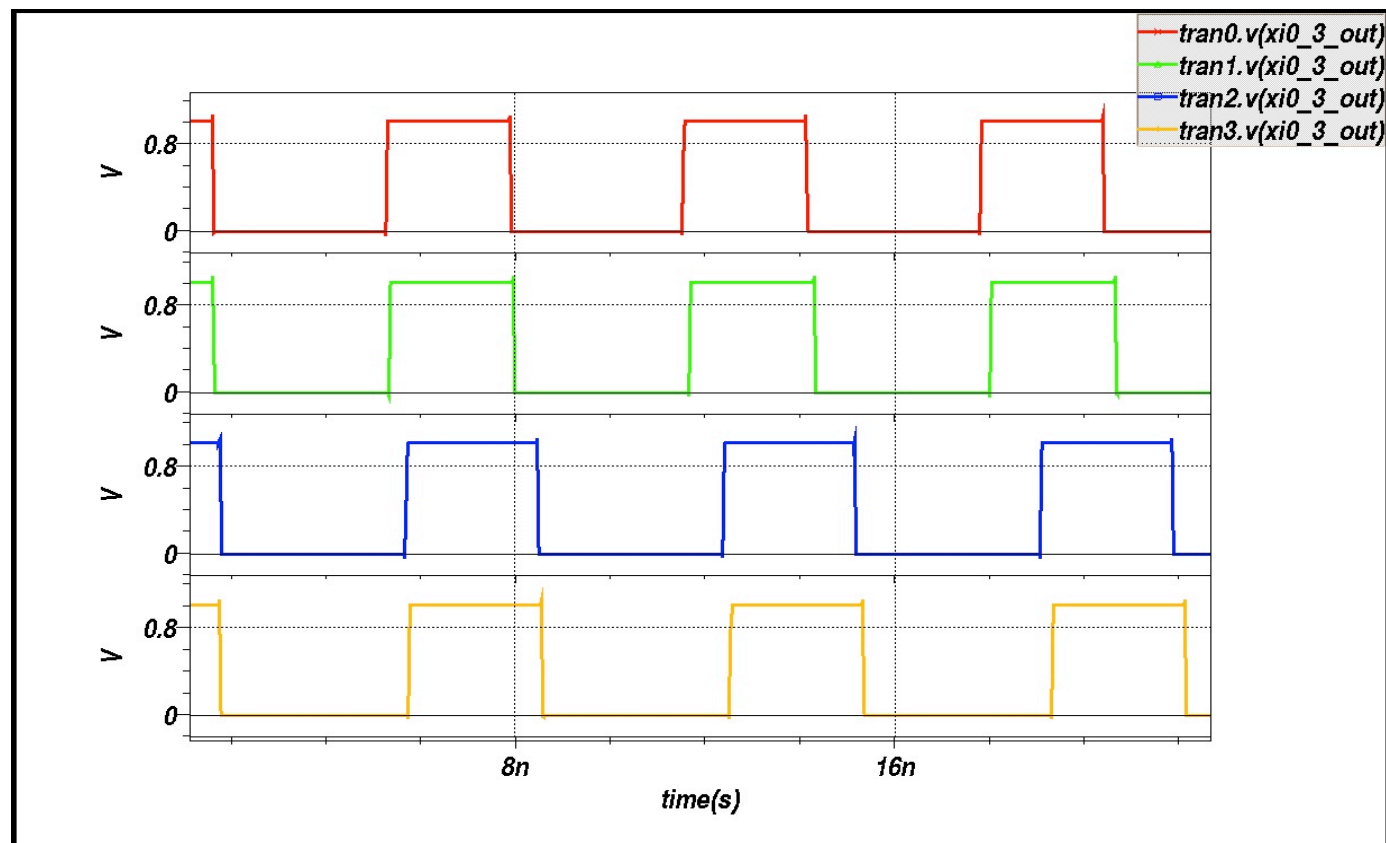
HIPEX-RC Simulation Results

Netlist without
parasitic
(HIPEX-Net)

R parasitic
netlist
(HIPEX-RC)

C parasitic
netlist
(HIPEX-C)

RC parasitic
netlist
(HIPEX-RC)



Delay is mostly caused by parasitic capacitance!



Overview

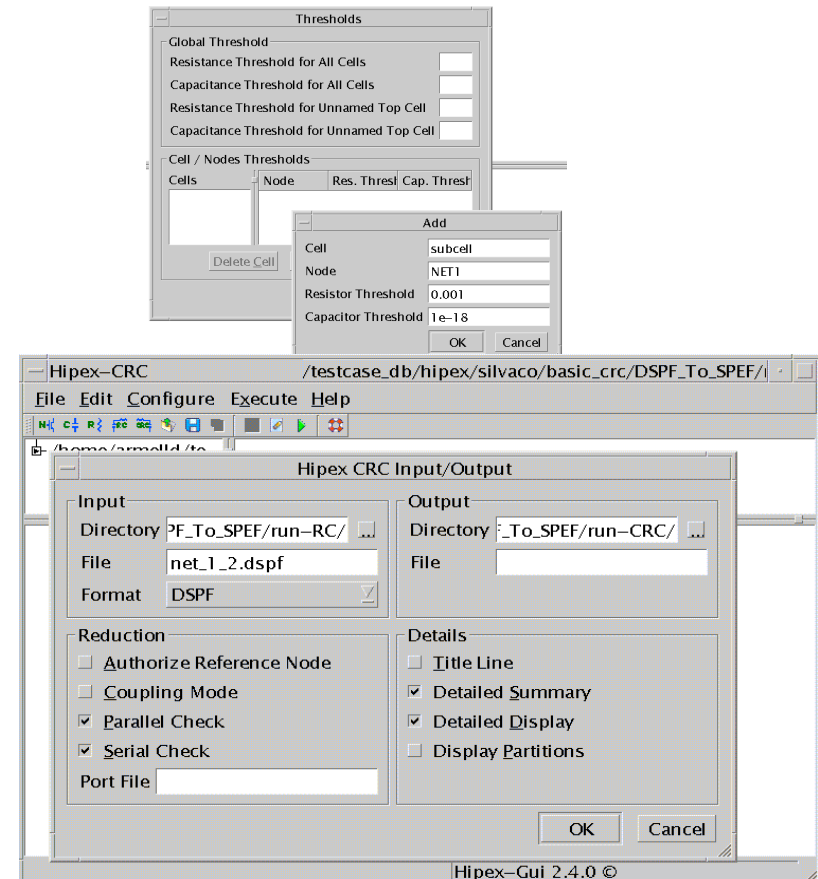
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HIPEX-CRC – Network Reduction Tool



HIPEX-CRC Overview

- Reduces RC netlists produced by major EDA parasitic extractors
- Excellent accuracy in reduced netlist due to advanced partitioning and pattern-matching based algorithm
- Supports main industry standards parasitic formats
- Final step of HIPEX-RC flow or as standalone tool
- Graphic User Interface provides control on HIPEX-CRC execution and settings





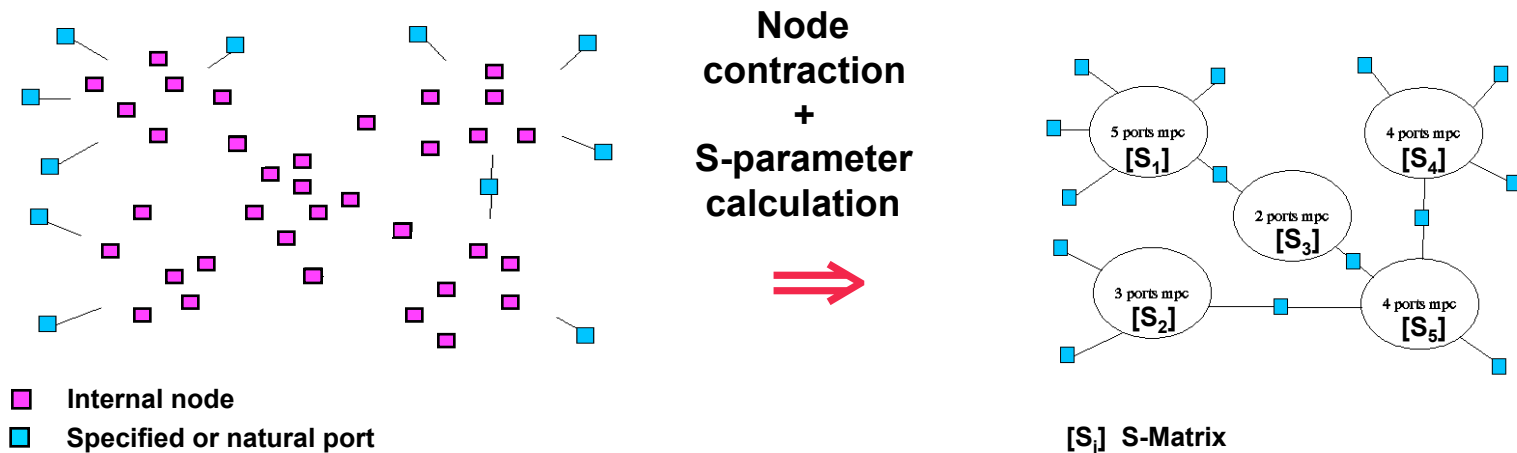
Key Capabilities

- **Reduction of any parasitic network**
 - Handles RC networks with loops
 - Handles coupling capacitors
- **Efficient reduction based on a combination of techniques**
 - Equivalent series and parallel merging
 - Dangling and floating nodes removal
 - Scattering-Parameter-Based Macromodeling

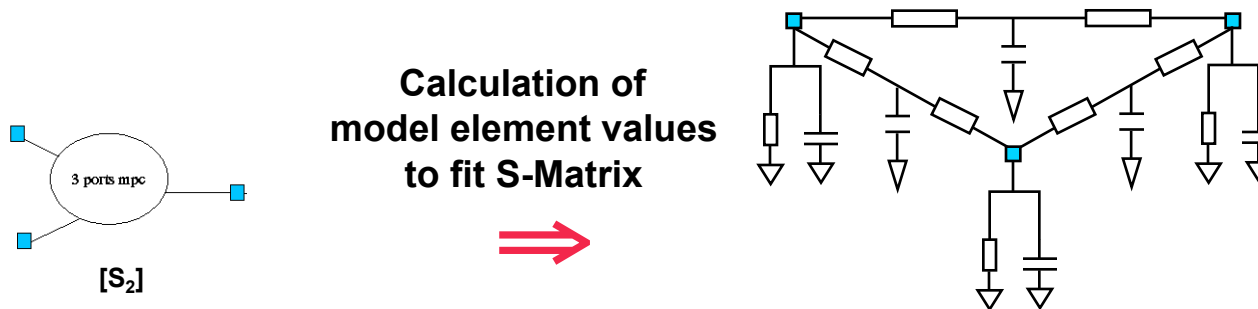


S-Parameter Based Reduction and Synthesis

Step 1 : node contraction and partitioning



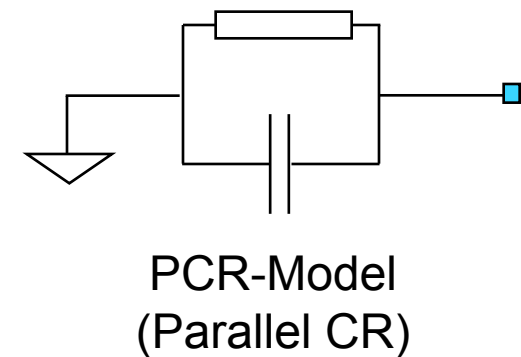
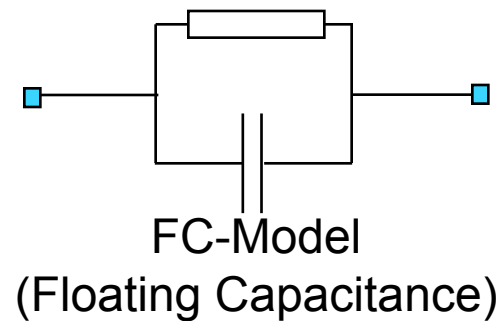
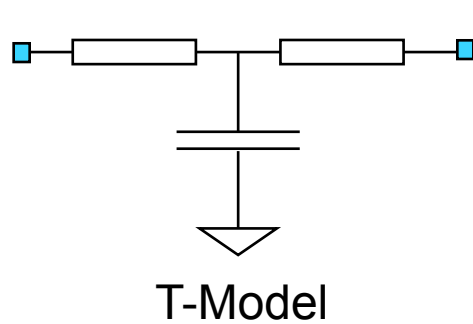
Step 2 : S-parameter based macromodeling





Realizable Model Reduction

Reduced RC networks are synthesized with the following patterns



Realizability of the reduced circuit equations enables back-end use of a variety of simulation and analysis tools



HIPEX-CRC Offers Full Set of Reduction Options

- Custom Reduction: a full set of options can be specified in the option file or through the GUI
 - IGNORE option, to skip user defined cells or SPF nets
 - THRESHOLD option, to enhance the reduction by suppressing negligible RC elements
 - SET_PORTS option, to specify additional irreducible nodes, and control circuit topology
 - SET_GROUND option, to specify ground net
 - REFERENCE_NODE option, to automatically set the macromodel reference node
 - PARALLEL/SERIES option, to enhance the reduction by prior merging parallel or series RC elements

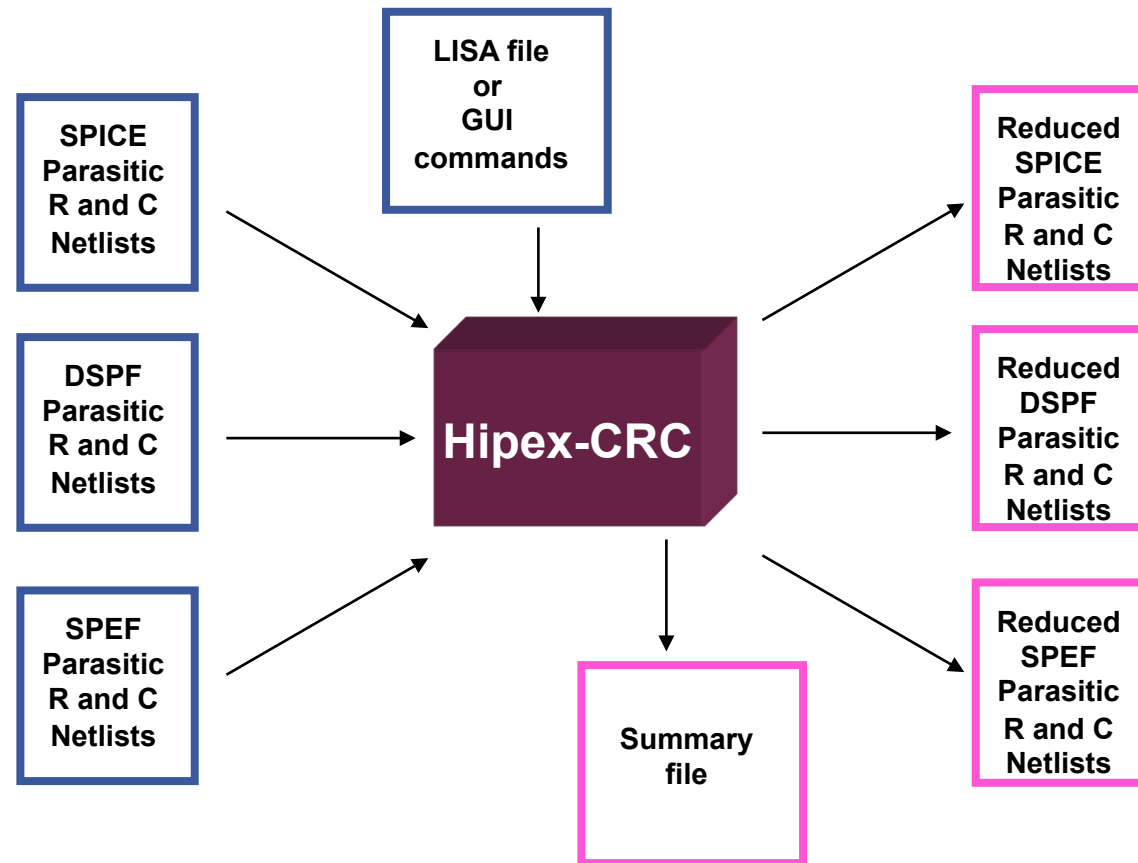


HIPEX-CRC Flexibility

- Netlist reader/writer supports various SPICE statements
 - Subcircuit definitions and calls to instances
 - MOSFET, MESFET, JFET, BJT transistors
 - Diodes
 - Passive devices (capacitor, resistor)
 - Independent voltage and current sources
- Acts on flat and/or hierarchical netlists, with automatic determination of ports
- Supports SPICE, DSPF and SPEF input and output formats
 - Integrated DSPF ' SPEF converter
 - Integrated SPEF ' DSPF converter } for direct input in different timing-analysis back-end tools



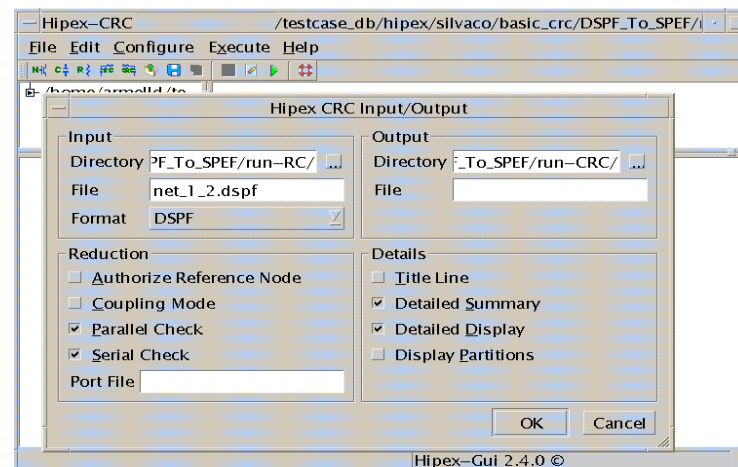
HIPEX-CRC Inputs/Outputs





HIPEX-CRC Outputs

- RC and devices reduced netlists
 - flat or hierarchical
 - DSPF, SPEF or SPICE formatted
- Detailed Summary File
 - Two levels of detail, selectable through the GUI
 - Number of device and RC parasitic elements per subcircuit or net
 - Number of resulting RC parasitic elements after each kind of reduction
 - Detailed partitioning of the circuit optionally displayed
 - Final reduction rate



```
Find: |
79 *I1 (m111402:d m111402 d x 0.000000 0.00 0.00)
80 *I1 (m181373:s m181373 s x 0.000000 0.00 0.00)
81 *I1 (m181372:g m181372 g x 0.000000 0.00 0.00)
82 *I1 (m111400:d m111400 d x 0.000000 0.00 0.00)
83
84 *R8 (5673:ADX19 0.00 0.00)
85 *R8 (5673:ADX18 0.00 0.00)
86 *R8 (5673:ADX17 0.00 0.00)
87 *R8 (5673:ADX16 0.00 0.00)
88 *R8 (5673:ADX15 0.00 0.00)
89 *R8 (5673:ADX14 0.00 0.00)
90 *R8 (5673:ADX13 0.00 0.00)
91 *R8 (5673:ADX12 0.00 0.00)
92 *R8 (5673:ADX11 0.00 0.00)
93 *R8 (5673:ADX10 0.00 0.00)
94
95 C10 5673:ADX10 vsss 0.000321106PF
96 R20 m181373:s 5673:ADX10 22.3401
97 R21 5673:ADX10 m111403:g 64.5179
98 C11 5673:ADX11 vsss 0.00033448PF
99 R22 m181373:s 5673:ADX11 21.6963
100 R23 5673:ADX11 m181372:g 56.1775
101 C12 5673:ADX12 vsss 0.000363547PF
102 R24 m181373:s 5673:ADX12 20.2713
103 R25 5673:ADX12 m111402:d 41.3841
104 C13 5673:ADX13 vsss 0.00036768PF
105 R26 m181373:s 5673:ADX13 20.2713
106 R27 5673:ADX13 m111400:d 41.3841
107 C14 5673:ADX14 vsss 0.000161435PF
108 R28 m111400:d 5673:ADX14 73.8319
109 R29 5673:ADX14 m111403:g 104.445
110 C15 5673:ADX15 vsss 0.000173583PF
111 R30 m111400:d 5673:ADX15 70.4651
112 R31 5673:ADX15 m181372:g 89.3717
113 C16 5673:ADX16 vsss 0.00029524PF
114 R32 m111400:d 5673:ADX16 0.00100003
115 R33 5673:ADX16 m111402:d 0.00100003
116 C17 5673:ADX17 vsss 0.000159582PF
117 R34 m111402:d 5673:ADX17 73.8319
118 R35 5673:ADX17 m111403:g 104.445
```

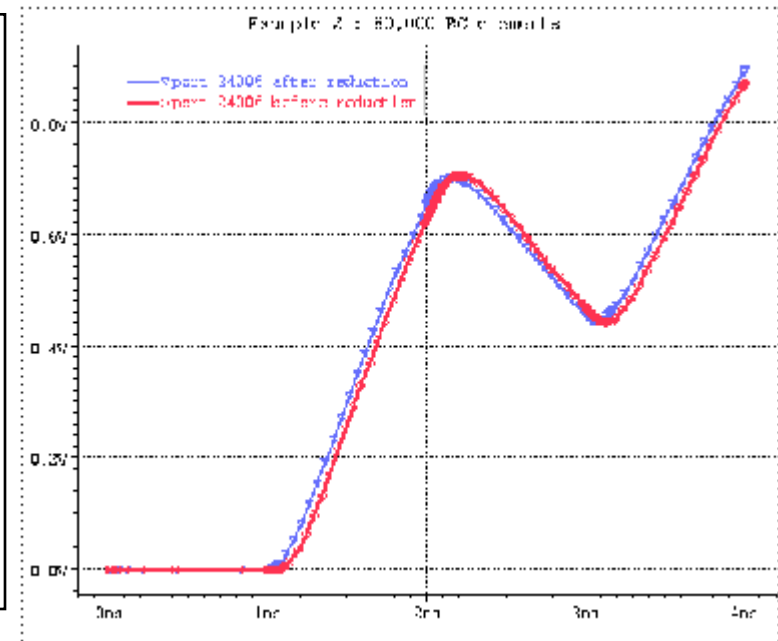
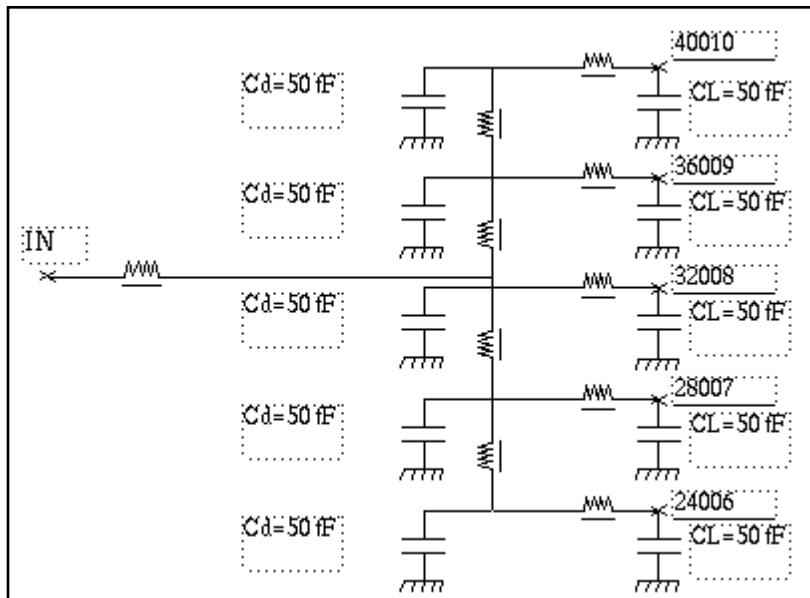


HIPEX-CRC Precision and Performance

- Performs networks reduction in linear time
- Preserves the same accuracy of simulation for reduced RC networks
- Significantly reduces runtime of post-layout and post-route simulations



Sample Test #1



Facts and figures

SPICE formatted netlist

of RC elements : 80,000

of ports : 6

% of reduction achieved : 99 %

Worst case voltage precision reached : 2.5 %

— After reduction
— Before reduction