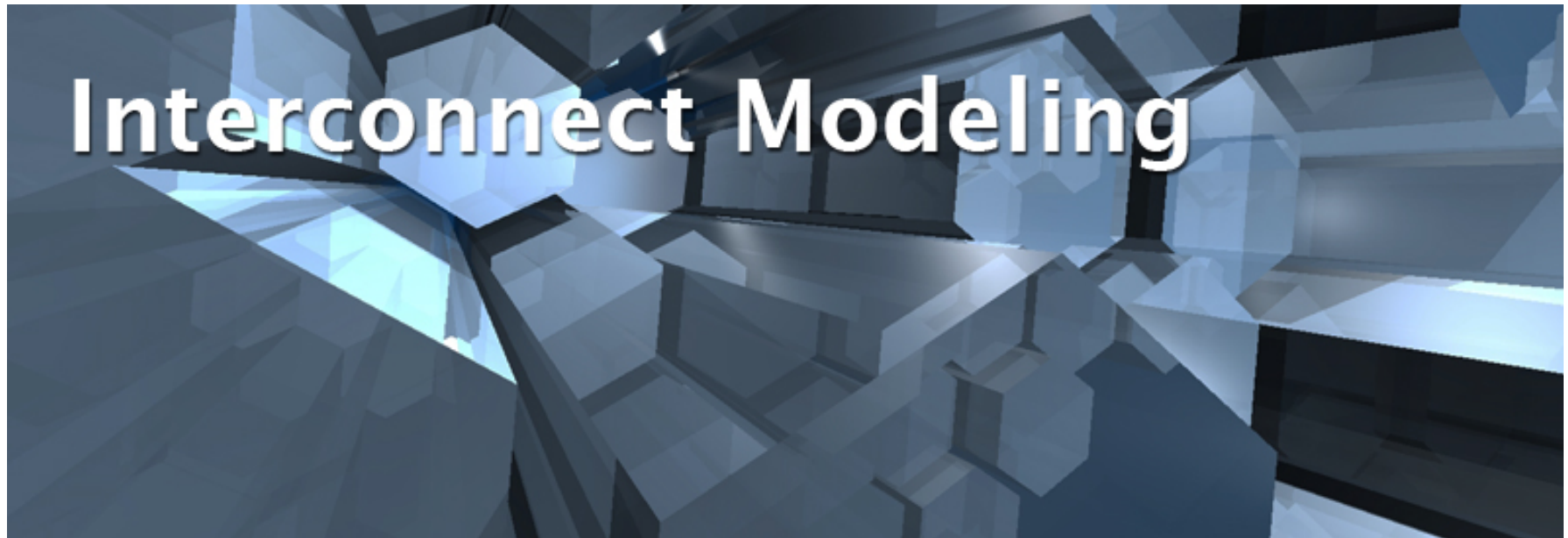


STELLAR –

Characterization of Standard Cell Parasitics



Competitive Summary



SILVACO

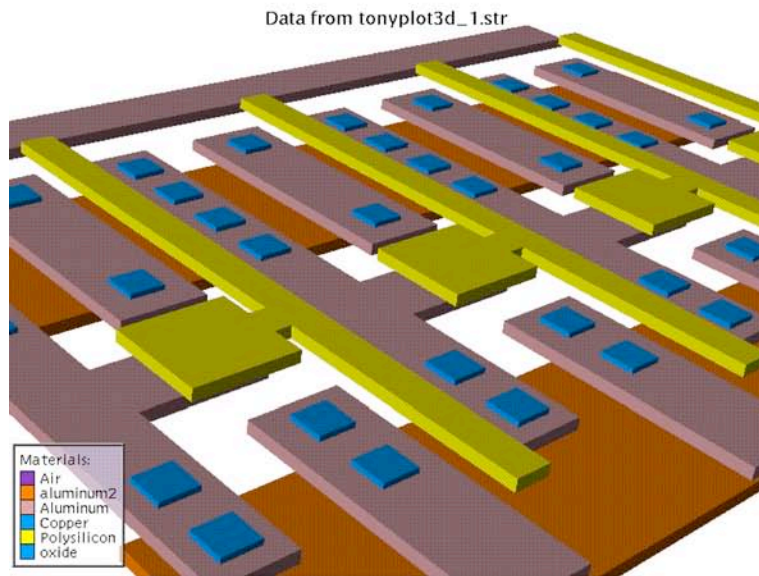
Interconnect Modeling

STELLAR – Competitive Summary

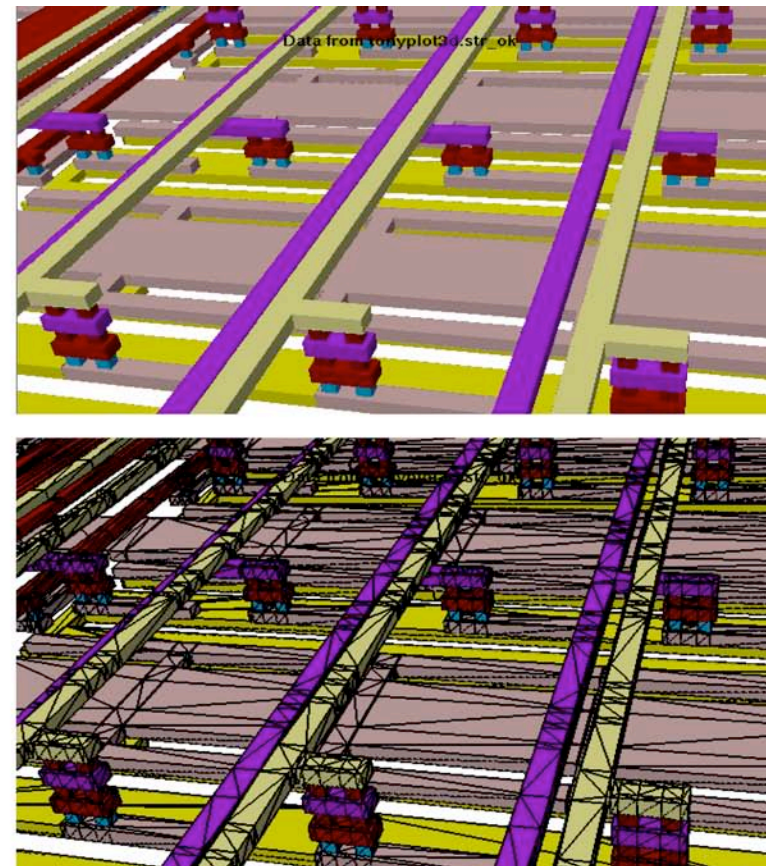
- Main Competitors:
 - Cell-AN (OEA International Inc)
 - QuickCap (Magma)
- STELLAR Advantages:
 - Pure physics capacitance extraction (100% field solver - not rule based)
 - Block level circuit size (100's of transistors in realistic time frames)
 - High accuracy
 - Built-in automated DOE features
 - Fast proprietary algorithms - Fictitious domain, Halo and Domain Decomposition
 - Automatic layout partitioning for fast parallel solving for larger circuits
 - Common GUI input to other Simucad parasitic tools

Interconnect Modeling

Pure Physics Capacitance Extraction (100% field solver - not rule based)



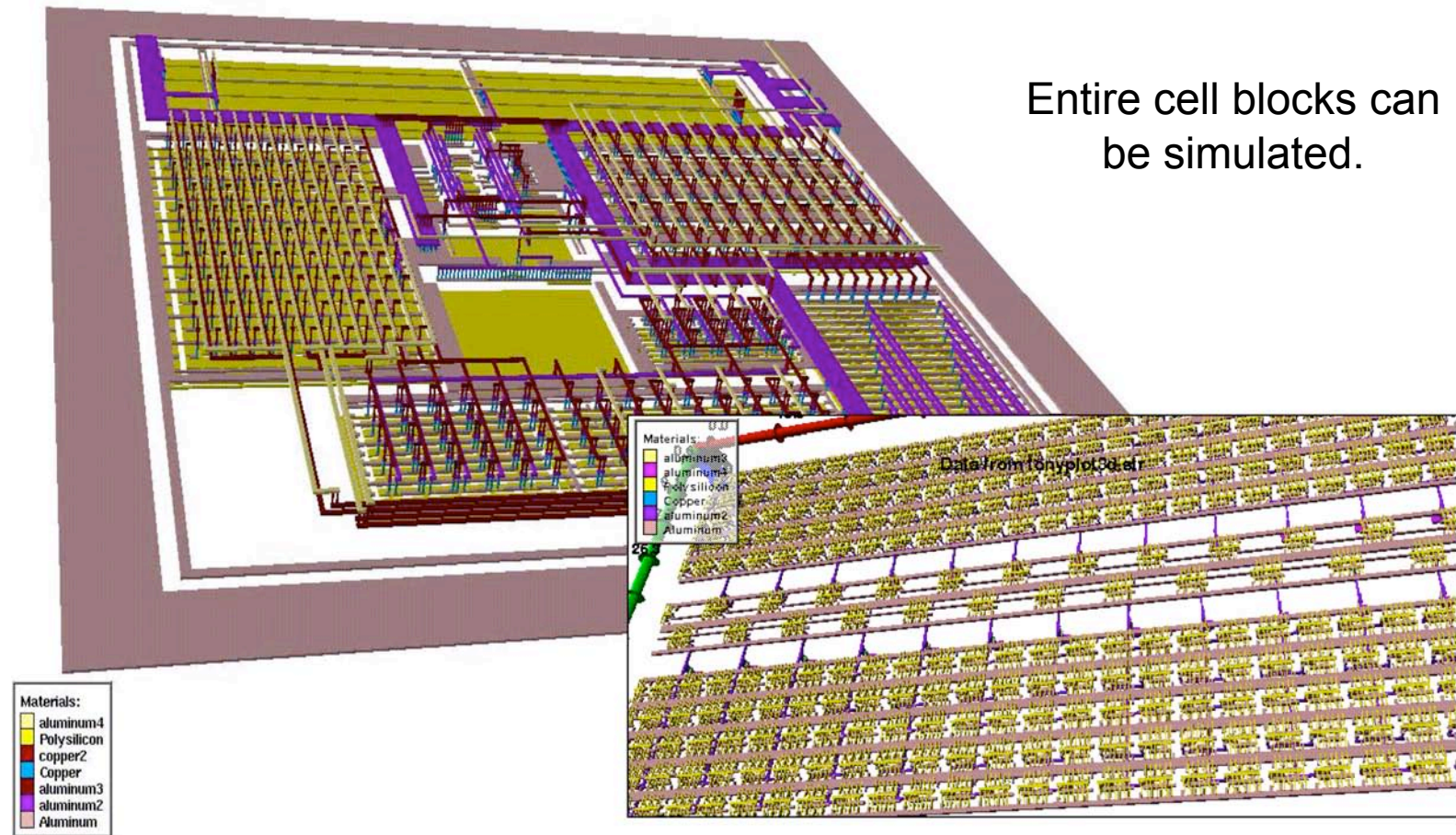
A complete 3D structure is created and field solved.



Interconnect Modeling

Block Level Circuit Size

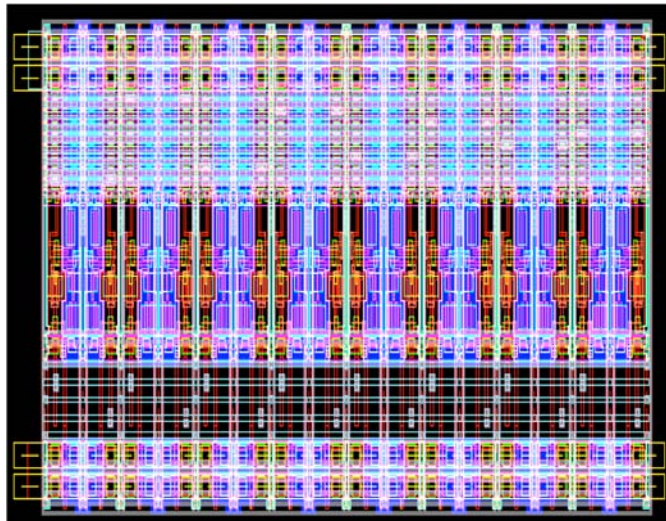
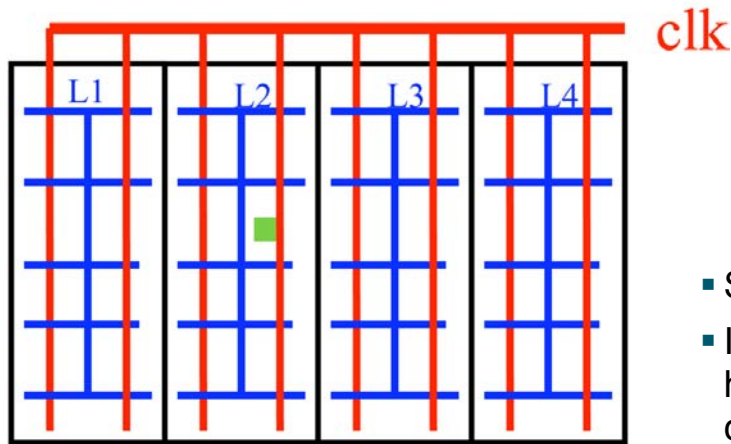
(100's of transistors in realistic time frames)



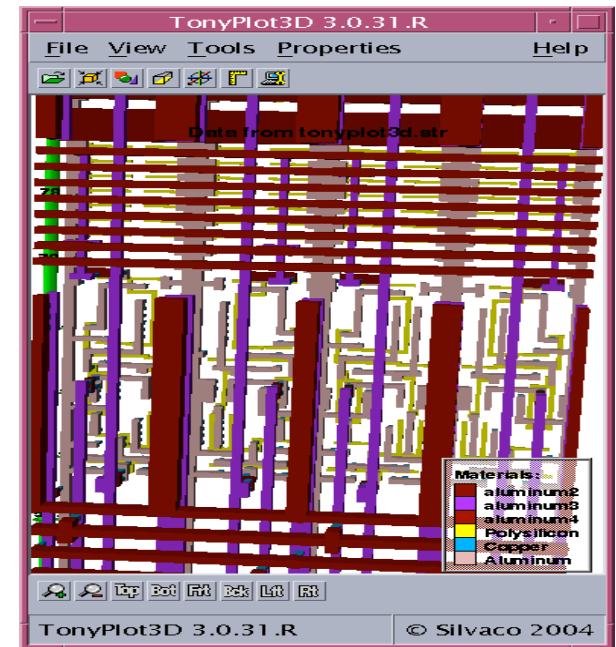
Entire cell blocks can be simulated.

Interconnect Modeling

Accuracy - Design Rule Checking Example



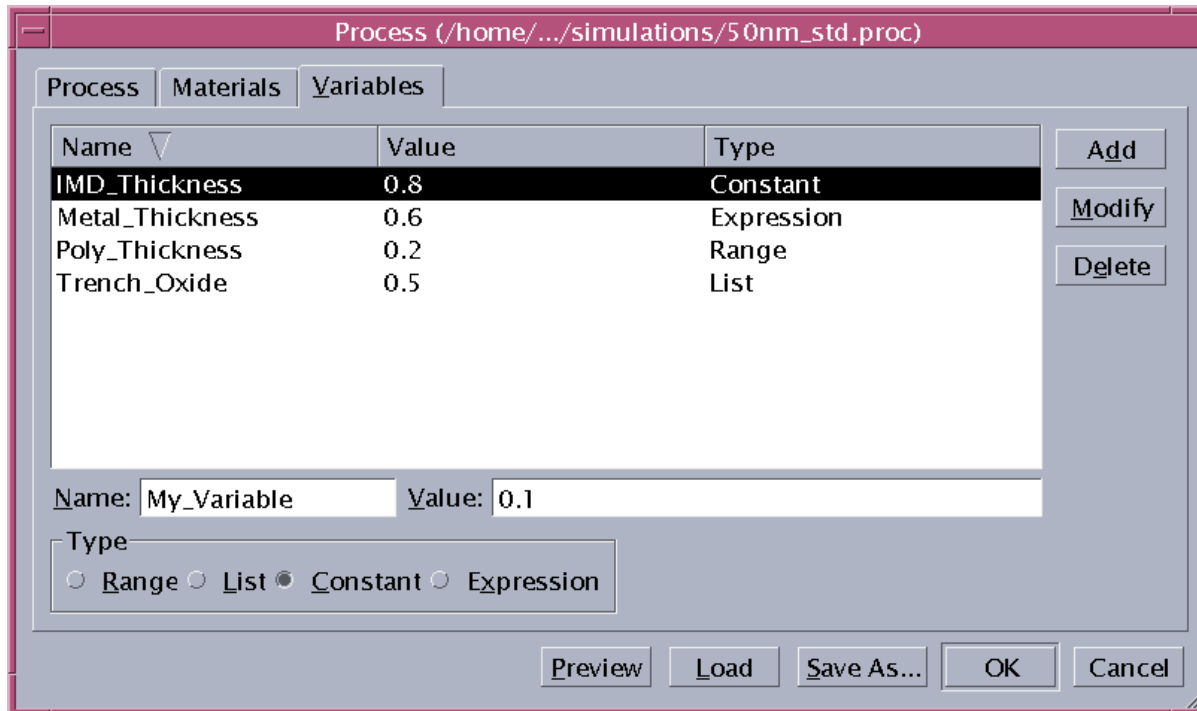
- Symmetrical layout
- Identical cells should have the same capacitances
- STELLAR detected layout error from capacitance variation



STELLAR is so accurate it can be used for design rule checking in repeated cell layouts.

Interconnect Modeling

Built-in Automated DOE Features



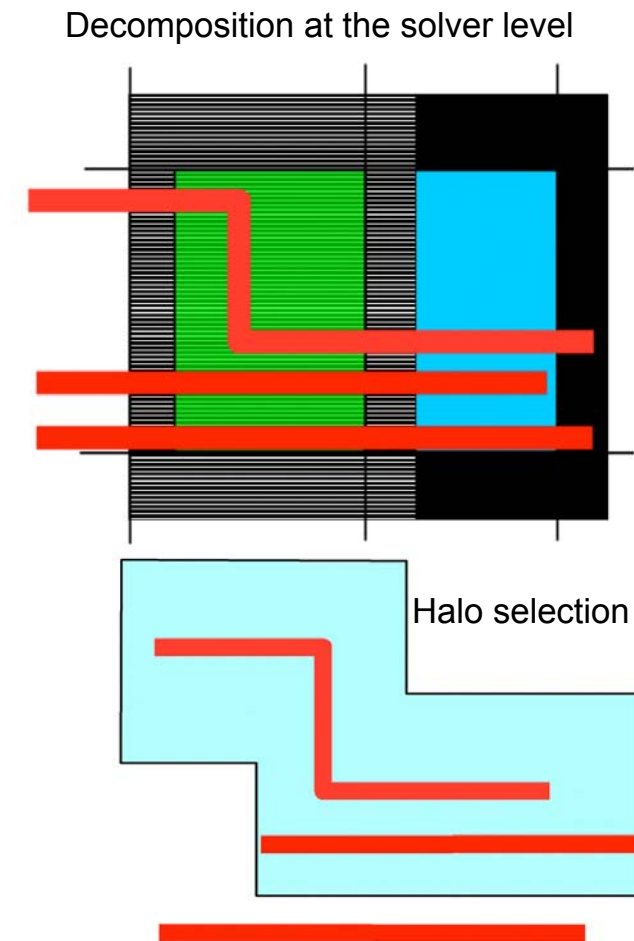
- STELLAR has a built-in DOE feature where ANY number of process or technology values can be a variable in the automated DOE and defined using the GUI based interface
- Ideal for process corner model investigation

Interconnect Modeling

Fast Algorithms - Fictitious Domain, Halo, Domain Decomposition

SUN-SPARC-V880 900 MHz	No Decomposition	Decomposition H=8 μ m
CPU (sec)	1300	600
Mem (GB)	1.200	0.200
C(F) in/out	14.04 10^{-14}	13.80 10^{-14}
in/substrate	12.46 10^{-14}	12.49 10^{-14}
out/substrate	9.63 10^{-14}	9.69 10^{-14}

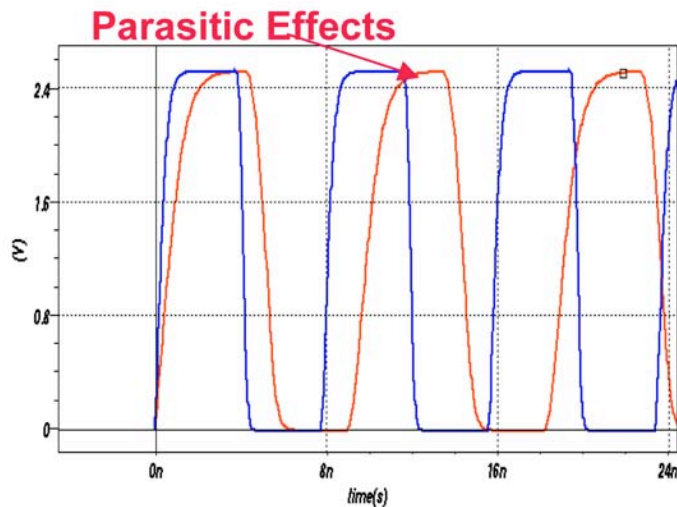
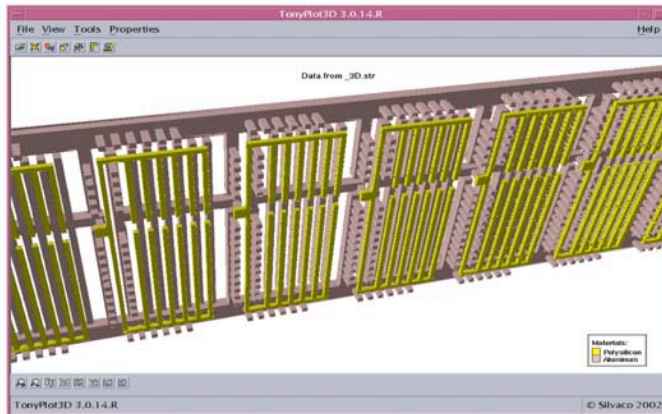
Fictitious domain, region of influence Halo and Domain Decomposition are all used for efficient, accurate capacitance extraction.



SILVACO

Interconnect Modeling

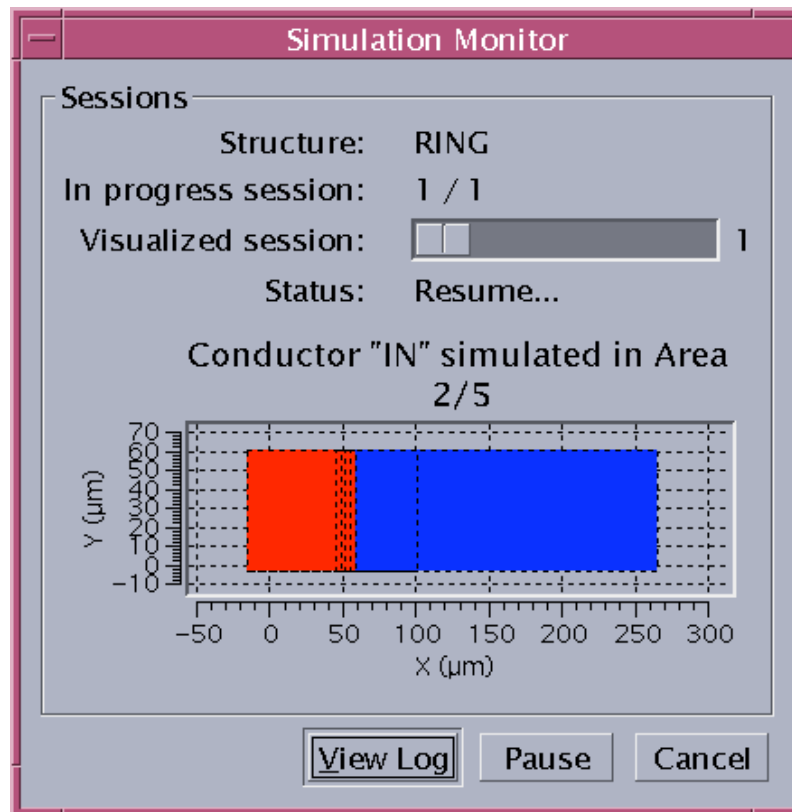
Fast Proprietary Algorithms – Measured Data Example



- Ring Oscillator spice simulation
 - Machine: Linux 64-bit, 2 GbyteRAM, cpu 2.4Ghz
 - 34 inverters simulated at the physical level (field solver)
 - Memory used : 666 MB for 34inverters
 - Simulation time : 730 seconds
 - Computed delay (in-out) : 6.95 ns
 - Measured delay (in-out) : 6.84 ns

Interconnect Modeling

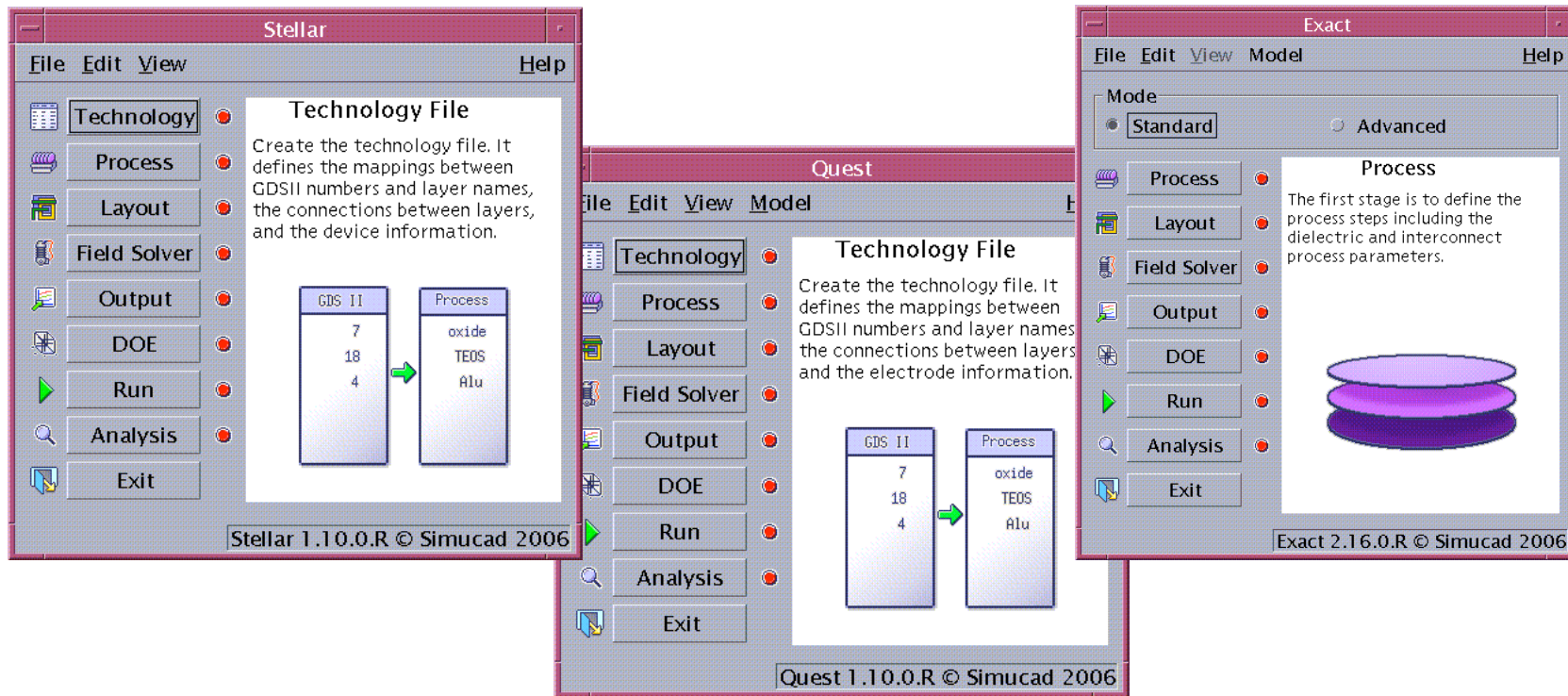
Automatic Layout Partitioning for Fast Parallel Solving for Larger Circuits



- STELLAR Partitions the Circuit and Displays Progress Status during Runtime

Interconnect Modeling

Common GUI Input to Other Simucad Parasitic Tools



For fast user familiarization with Simucad parasitic tools, a common GUI interface is used.

Interconnect Modeling

Buy STELLAR for Accurate Characterization of CustomCell Blocks or Back End Corner Model Analysis

- STELLAR is the solution for 90nm and below technologies when very accurate parasitic extraction on custom cell blocks is required because:
 - 100% physics based capacitance solver
 - Any number of process technology parameters can be used as a variable for design optimization and corner modeling
 - Efficient solver techniques allow large cell blocks to be accurately characterized in a timely manner
 - Easy to use GUI interface