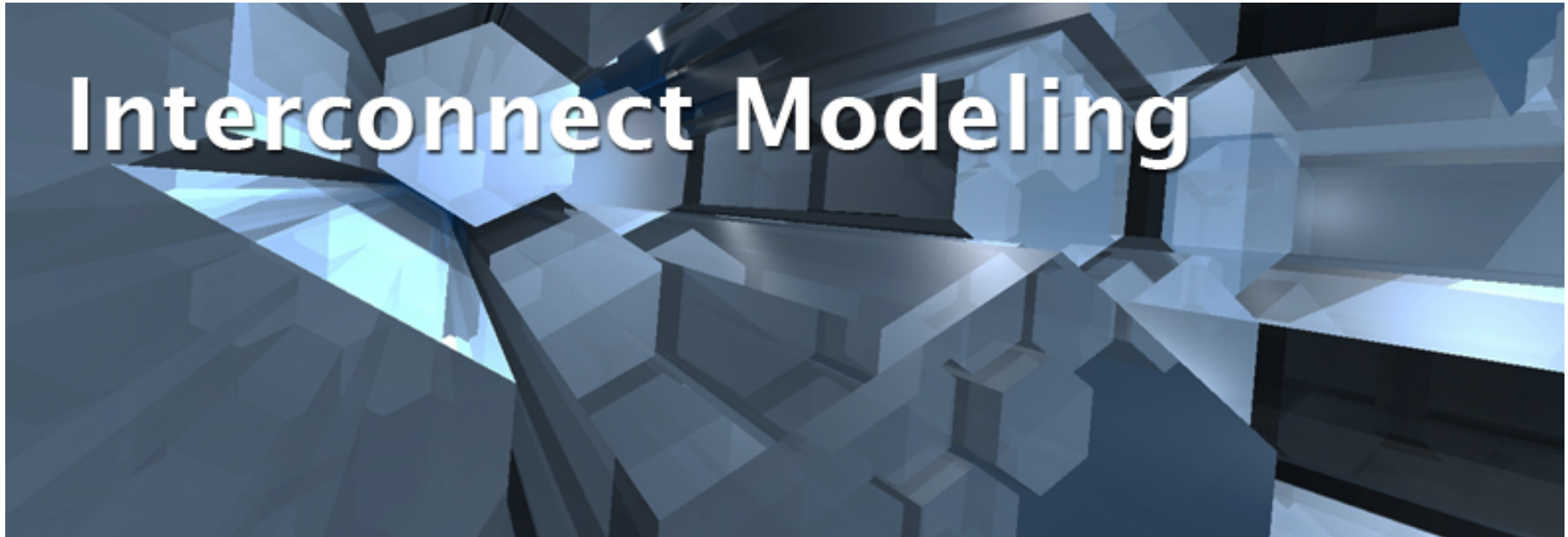


STELLAR

Cell Process-Based 3D Capacitance Extractor



Unique, Advanced, TCAD Based Parasitic Extractor



SILVACO

Interconnect Modeling

Outline

- What is Stellar
- Inputs/Outputs
- Specific Capabilities
- STELLAR GUI
 - Derived Layer
 - Device Setup
- Output
 - 3D structure
 - Spice Netlist
 - Spice Simulation
- Conclusion

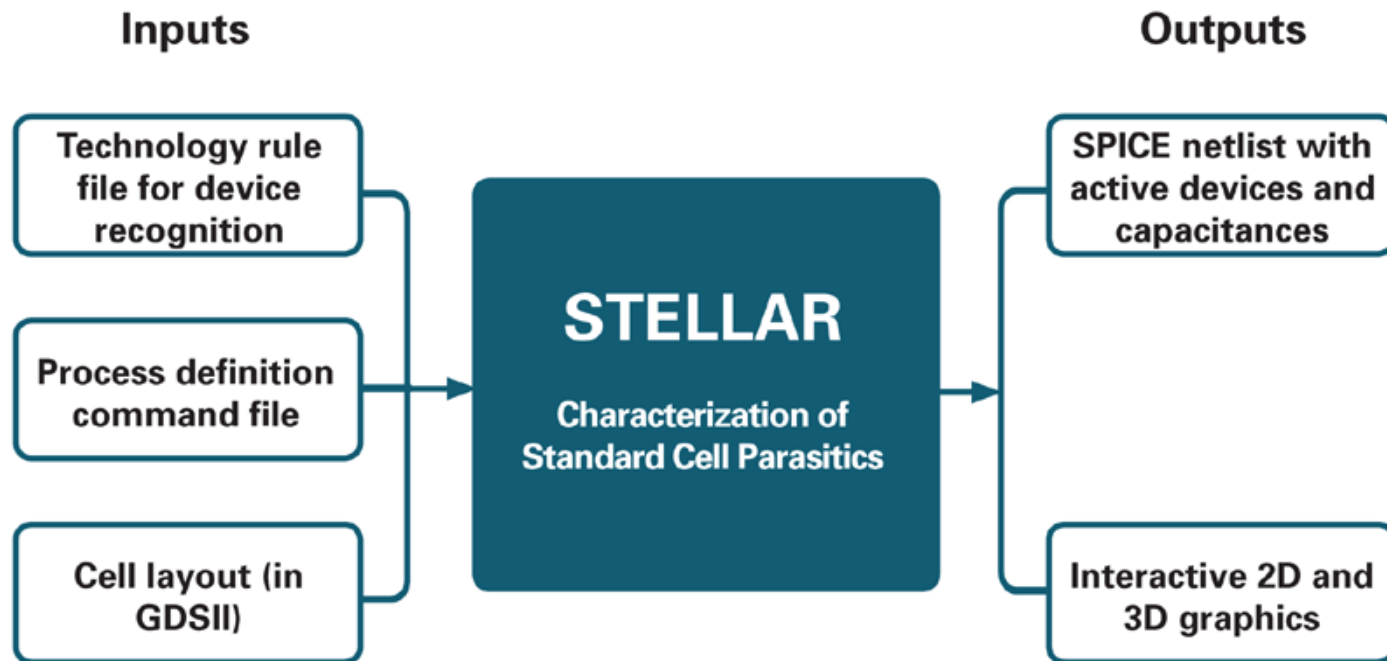
Interconnect Modeling

What is STELLAR?

- 3D Capacitance extractor on large chips
- High accuracy
- Efficient 3D Field Solver based on The Fictitious Domains Method
- Intuitive and user-friendly graphical interface
- Direct Spice netlist extraction
- Integrated scripting language

Interconnect Modeling

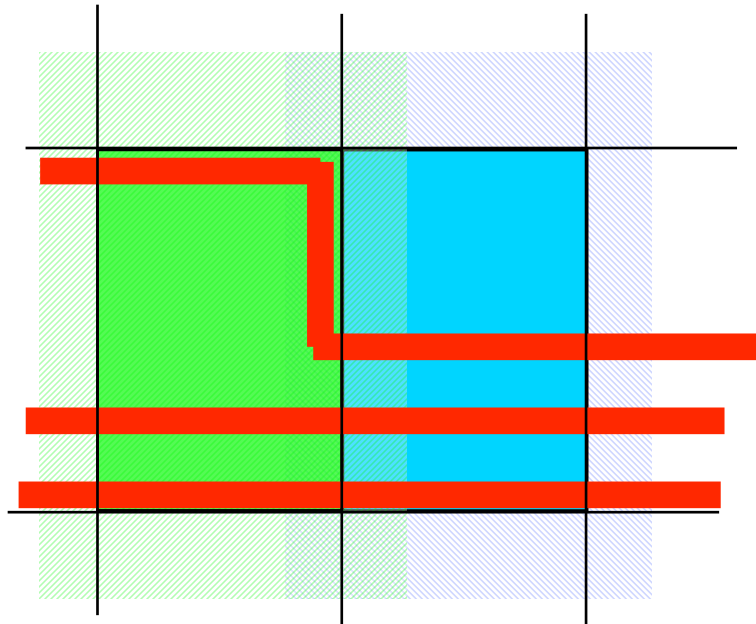
STELLAR Inputs/Outputs



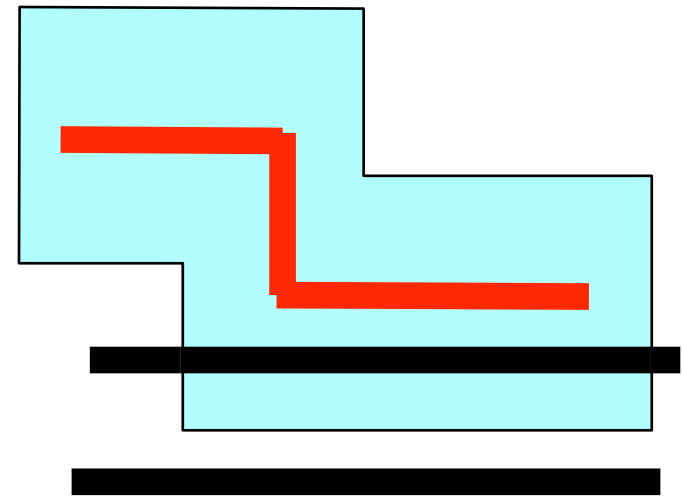
Interconnect Modeling

Specific Simulation Capabilities

Domain Decomposition



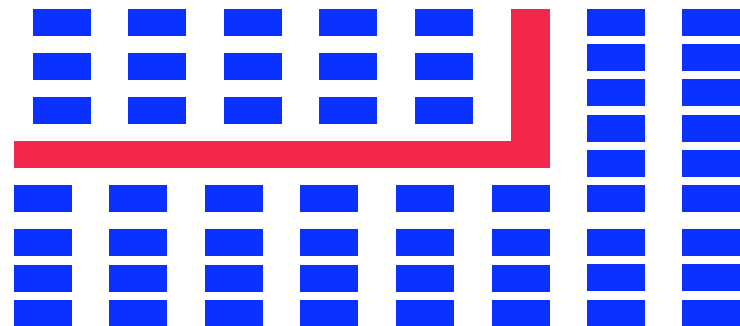
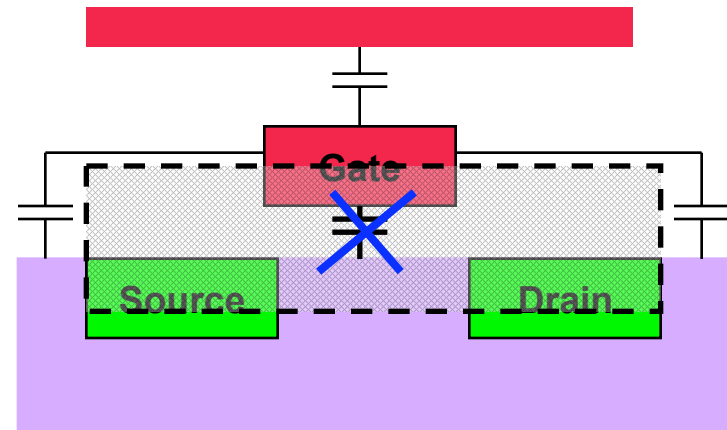
HALO Selection



Interconnect Modeling

Specific Simulation Capabilities (con't)

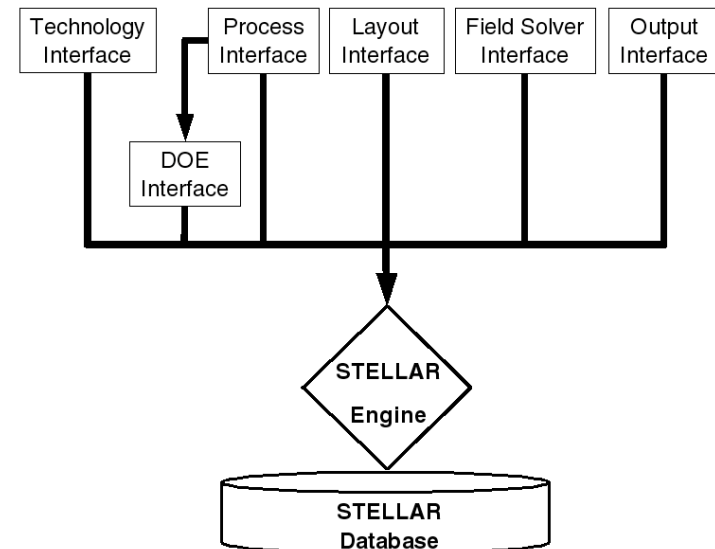
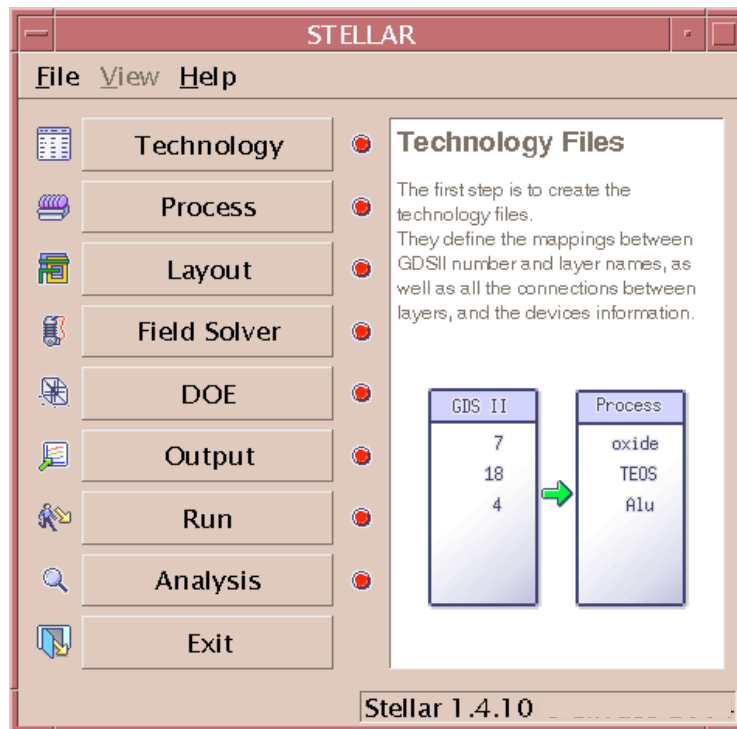
- Gate capacitance extraction
- Structures with floating conductors
- Stop and Restart a simulation



Interconnect Modeling

STELLAR GUI

- Same Graphical User Interface as compared to QUEST and EXACT



Interconnect Modeling

Technology Step: Derived Layer Definition

Techno

General | Layer Setup | Connection Setup | Device Setup

Mappings

	GDSII Number	GDSII Datatype	Layer Name	Text	Derived Layer
1	10	0	VIA1	No	No
2	8	0	CONT	No	No
3	23	0	CONT_WELL	No	No
4	12	0	CONT_BULK	No	No
5	9	0	ME1	No	No
6	5	0	POLY	No	No
7	11	0	ME2	No	No
8	21	0	NACT	No	No
9	22	0	PACT	No	No
10	1	0	NWELL	No	No
11	9	1	ME1_TXT	Yes	No
12	11	1	ME2_TXT	Yes	No
13	5	1	POLY_TXT	Yes	No
14	-1	-1	PGATE	No	Yes
15	-1	-1	NGATE	No	Yes
16	-1	-1	PSD	No	Yes
17	-1	-1	NSD	No	Yes
18	-1	-1	BULK	No	Yes
19	-1	-1	SUBS	No	Yes

Add Layer | Delete Layer | Import GDS Data

Edit Derivation

OK | Load | Save As... | Cancel

Derived Layer Definition

Operation

- AND
- OR
- XOR
- DIF
- Resize
- Select
- Intersect
- Substrate

Input Layers

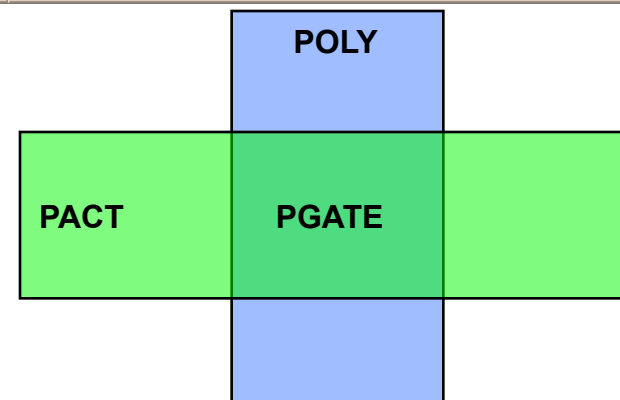
Layer 1: PACT

Layer 2: POLY

Output Layer(s)

Layer R: PGATE

Help | OK | Cancel

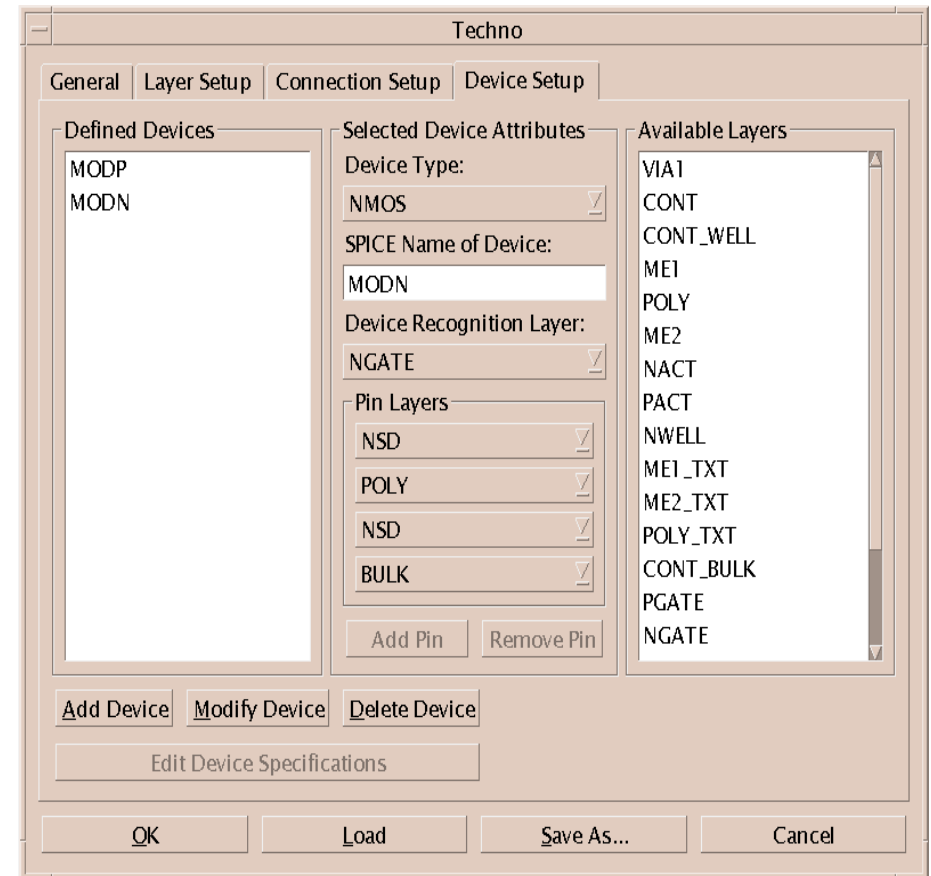
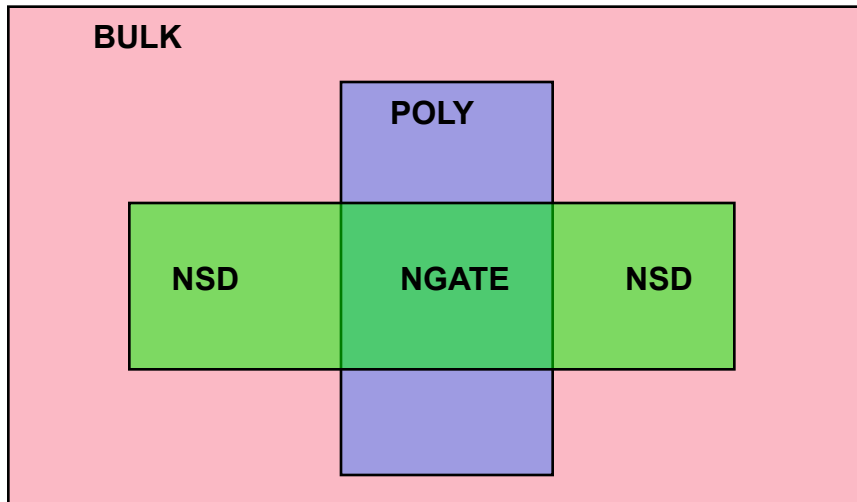


SILVACO

Interconnect Modeling

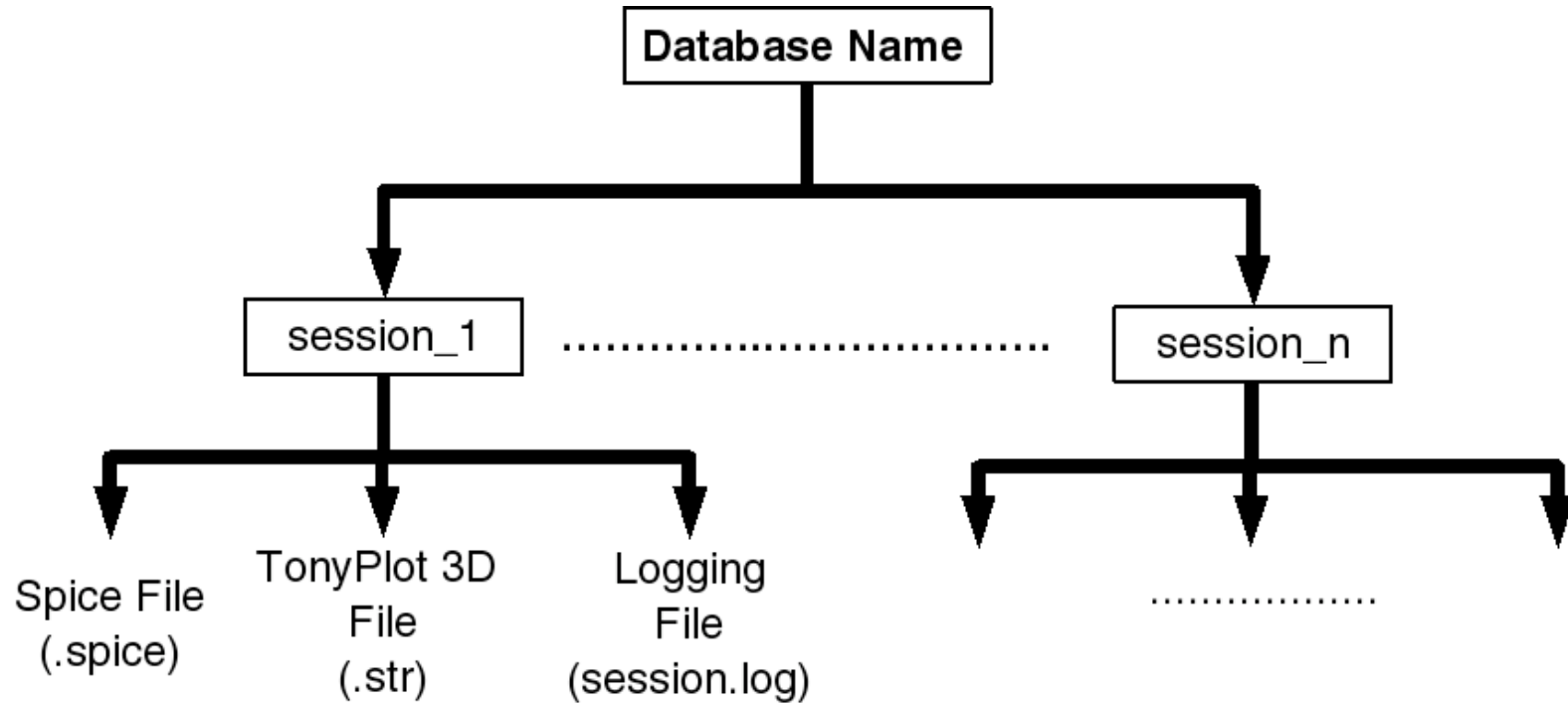
Technology Step: Device Setup

- Device extraction is BASED on the powerful HIPEX full chip extractor
- Extraction of all active and passive devices (MOS, BIP, Diodes, R, C...)
- Extraction of custom devices



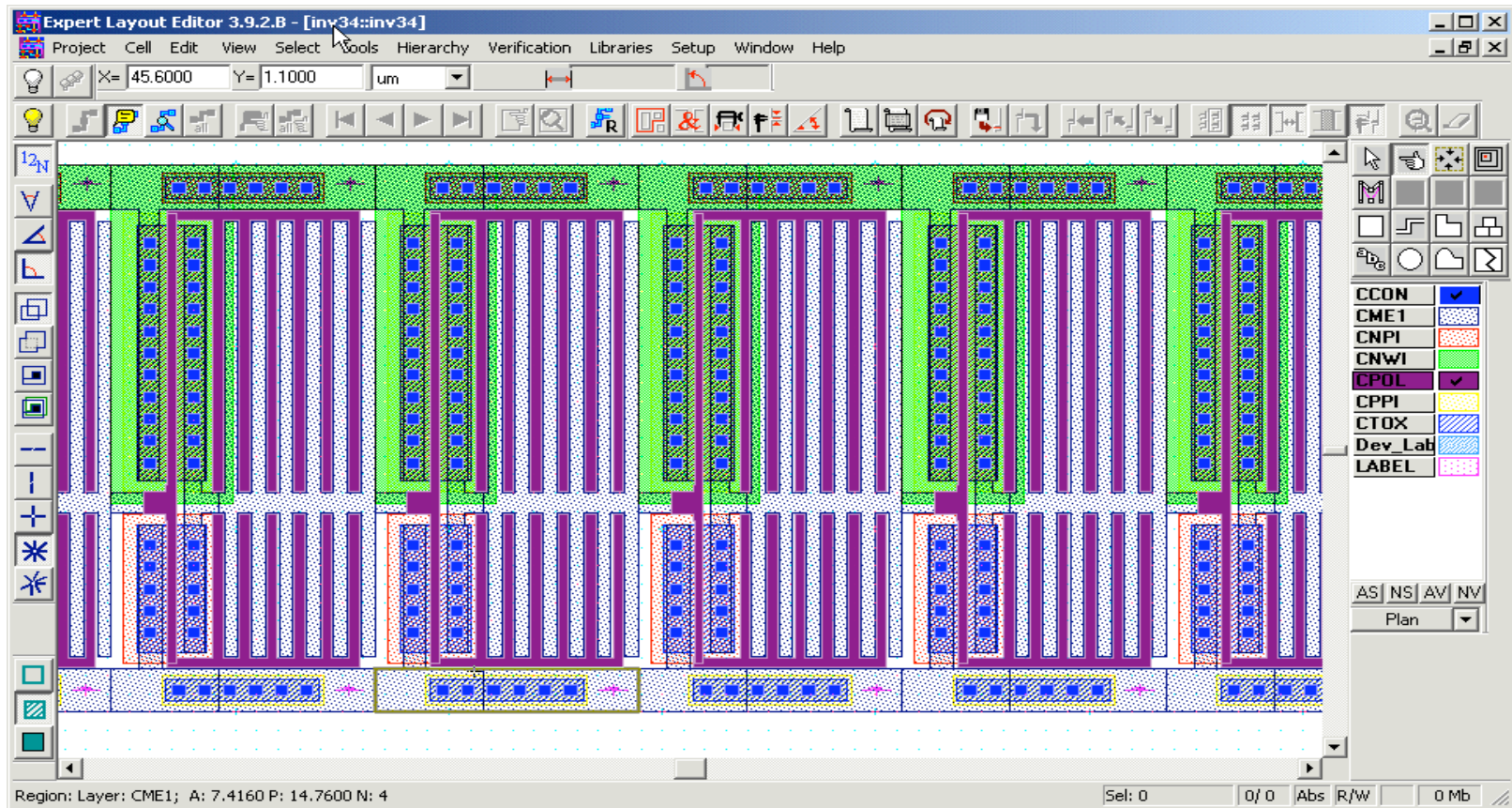
Interconnect Modeling

Architecture Of Output Data Storage



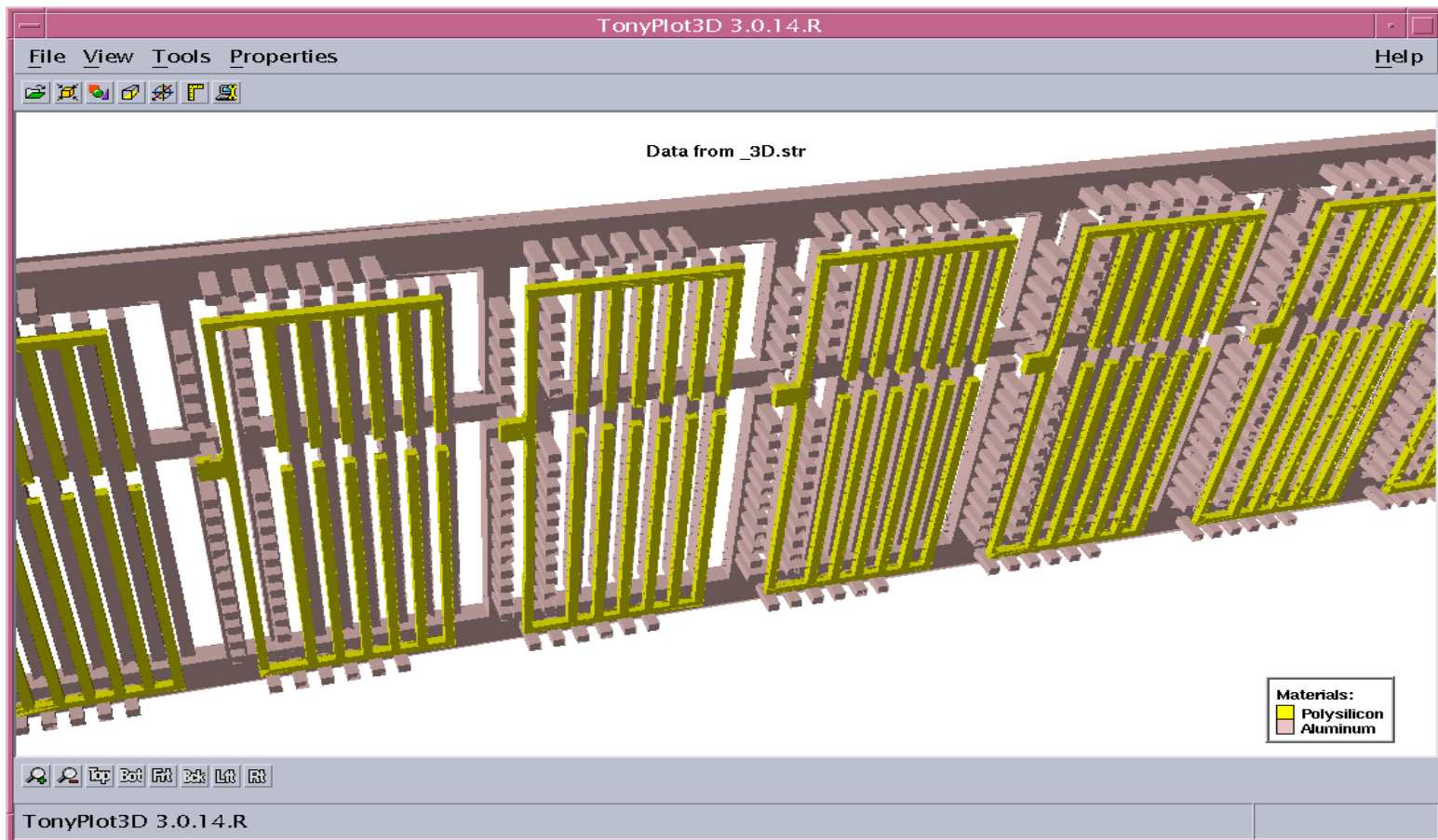
Interconnect Modeling

Example: Layout of a Chain of 34 Inverters



Interconnect Modeling

Example: 3D Interconnect Structure (dielectric layers hidden)



Interconnect Modeling

Example: Full Spice Netlist

Device
Extraction

Capacitance
Extraction

```
netlist.spice (/mnt/fannys/stel...sts/tutorial/db/session_1) - GVIM
File Edit Tools Syntax Buffers Window Help
SPICE netlist for MUX1
.global GND IN0 OUT SEL IN1 VDD
.MODEL MODN NMOS
.MODEL MODP PMOS
*****
* Sub-Circuit Netlist Of : MUX1
*****
MI7 2 SEL GND GND MODN L=2U W=10U AD=60P AS=60P PD=22U PS=22U
MI6 3 IN0 11 GND MODN L=2U W=24U AD=144P AS=24P PD=36U PS=2U
MI5 11 2 GND GND MODN L=2U W=24U AD=24P AS=144P PD=2U PS=36U
MI4 10 3 OUT GND MODN L=2U W=24U AD=24P AS=144P PD=2U PS=36U
MI3 GND 4 10 GND MODN L=2U W=24U AD=144P AS=24P PD=36U PS=2U
MI2 9 SEL 4 GND MODN L=2U W=24U AD=24P AS=144P PD=2U PS=36U
MI1 GND IN1 9 GND MODN L=2U W=24U AD=144P AS=24P PD=36U PS=2U
MI14 2 SEL VDD VDD MODP L=2U W=19U AD=114P AS=114P PD=31U PS=31U
MI13 3 2 VDD VDD MODP L=2U W=23U AD=73.6P AS=128.8P PD=6.4U PS=34.2U
MI12 VDD IN0 3 VDD MODP L=2U W=23U AD=138P AS=73.6P PD=35U PS=6.4U
MI11 VDD 4 OUT VDD MODP L=2U W=23U AD=128.8P AS=73.6P PD=34.2U PS=6.4U
MI10 OUT 3 VDD VDD MODP L=2U W=23U AD=73.6P AS=138P PD=6.4U PS=35U
MI9 4 SEL VDD VDD MODP L=2U W=23U AD=73.6P AS=138P PD=6.4U PS=35U
MI8 VDD IN1 4 VDD MODP L=2U W=23U AD=128.8P AS=73.6P PD=34.2U PS=6.4U
C0 SEL substrate 2.898849e-14
C1 VDD substrate 2.422772e-14
C2 GND substrate 2.054106e-14
C3 3 substrate 1.768967e-14
C4 4 substrate 1.765616e-14
C5 2 substrate 1.432217e-14
C6 4 VDD 1.234791e-14
C7 2 VDD 1.219009e-14
C8 4 GND 1.056423e-14
C9 3 VDD 1.036188e-14
C10 GND OUT 9.166939e-15
C11 3 GND 8.914418e-15
C12 IN1 substrate 7.950295e-15
C13 VDD OUT 7.694627e-15
C14 IN0 substrate 7.652883e-15
C15 OUT substrate 6.934699e-15
C16 2 GND 6.812382e-15
C17 3 OUT 6.323654e-15
C18 VDD SEL 4.842486e-15
C19 4 SEL 4.793325e-15
C20 3 IN0 4.518356e-15
C21 IN1 VDD 3.715930e-15
C22 GND SEL 2.592225e-15
C23 IN1 GND 2.487187e-15
C24 IN0 VDD 2.024495e-15
C25 2 SEL 1.823847e-15
1,1 Top
```

SmartSpice
Simulation

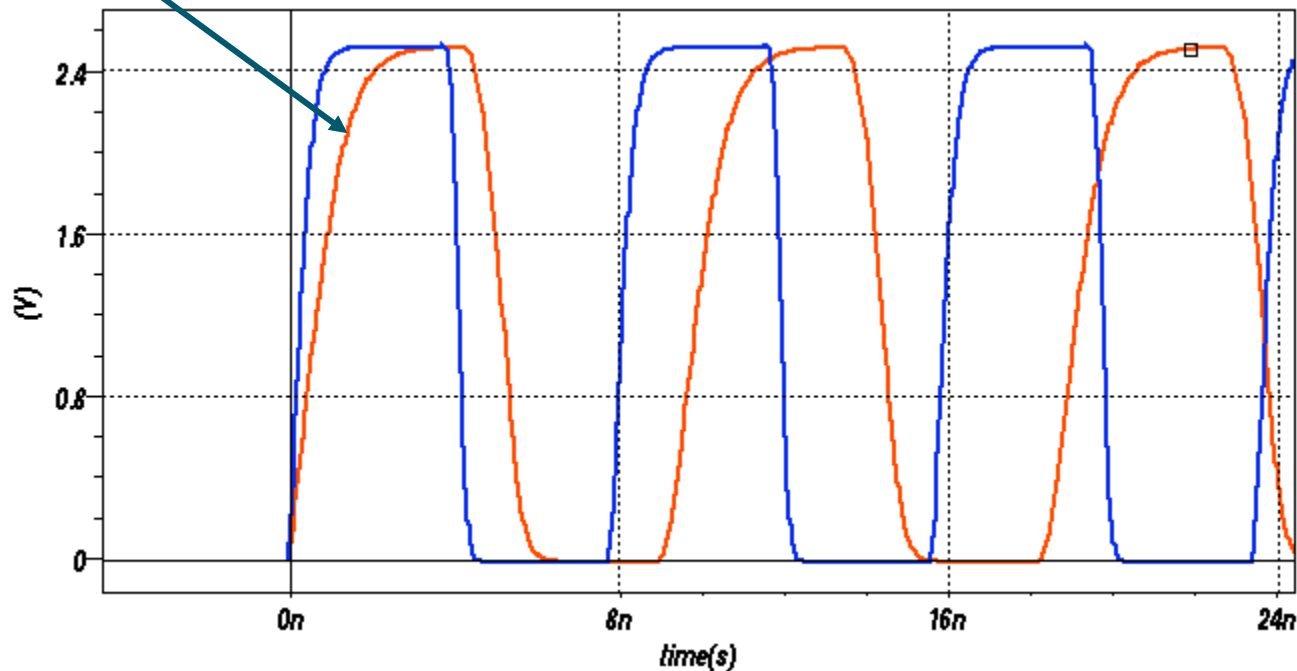
Spice Netlist File

Interconnect Modeling

Example: SmartSpice Simulation

- Ring Oscillator simulation with and without parasitics

Parasitics Effects



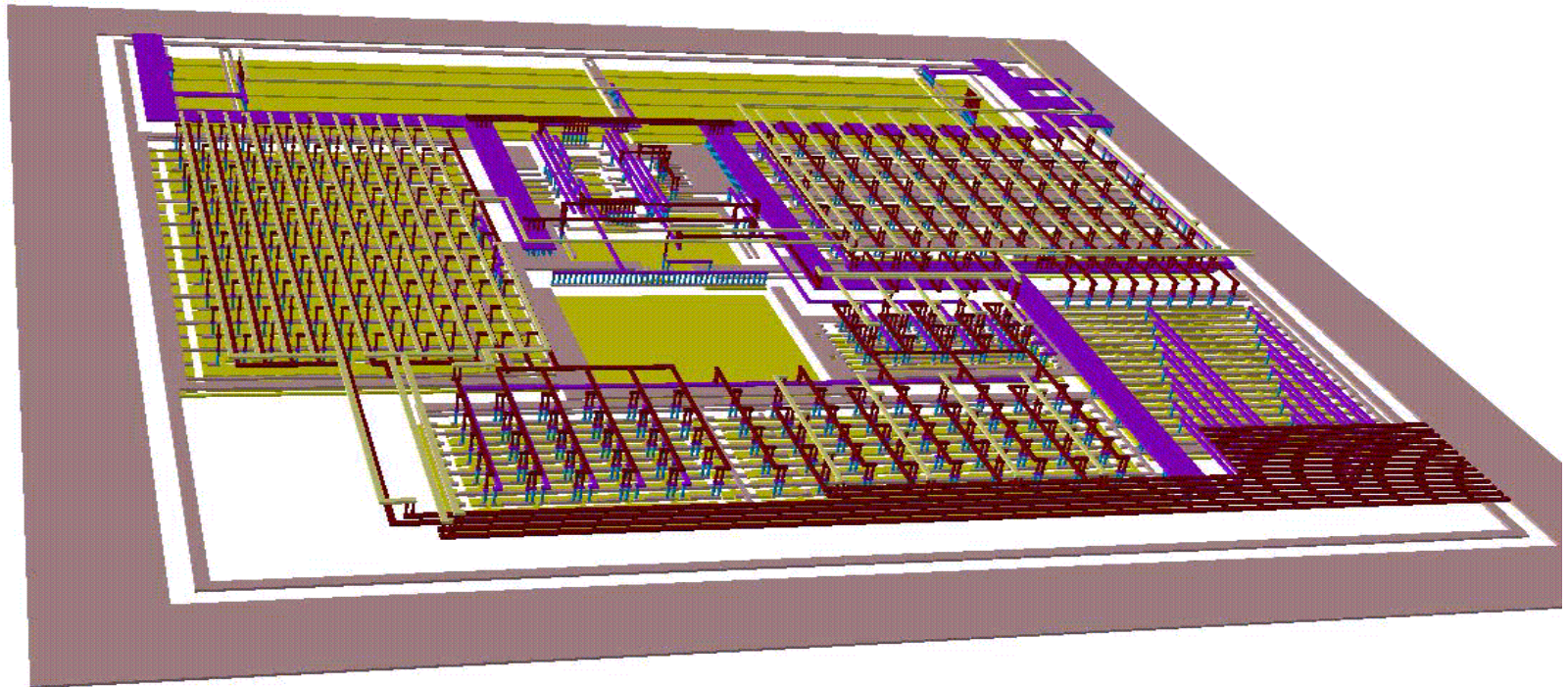
Interconnect Modeling

Example: Simulation Results

- Machine used for these simulations : SUN Ultra 10, 1Gig RAM
- STELLAR : 34 inverters simulated at the physical level (field solver)
- Memory used : 748.55 MB for 34 inverters
- Simulation time : 1894 seconds
- Computed delay (in-out) : 6.95 ns
- Measured delay (in-out) : 6.84 ns

Interconnect Modeling

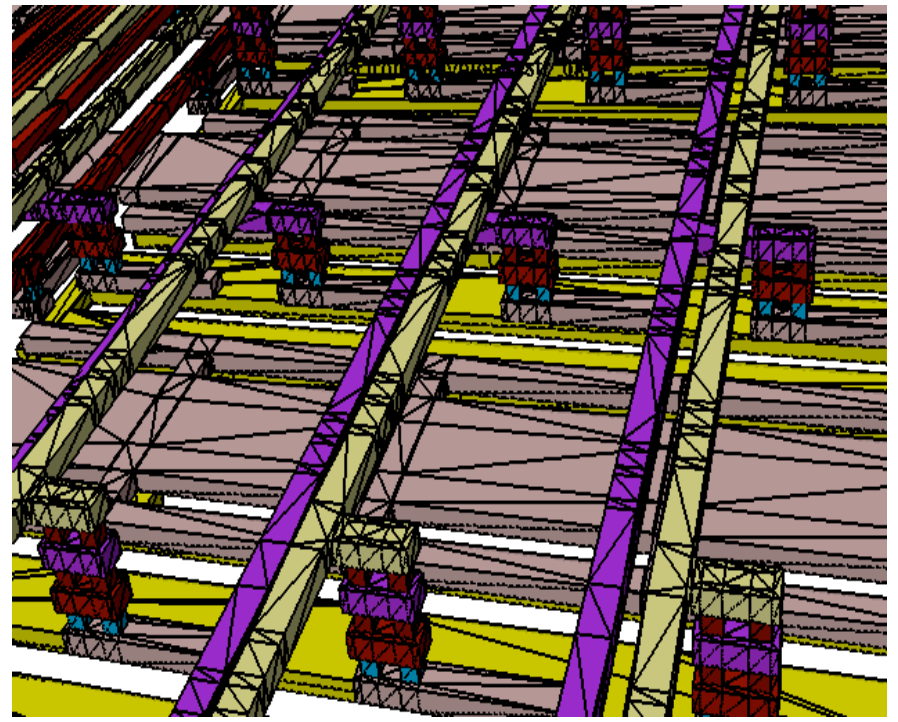
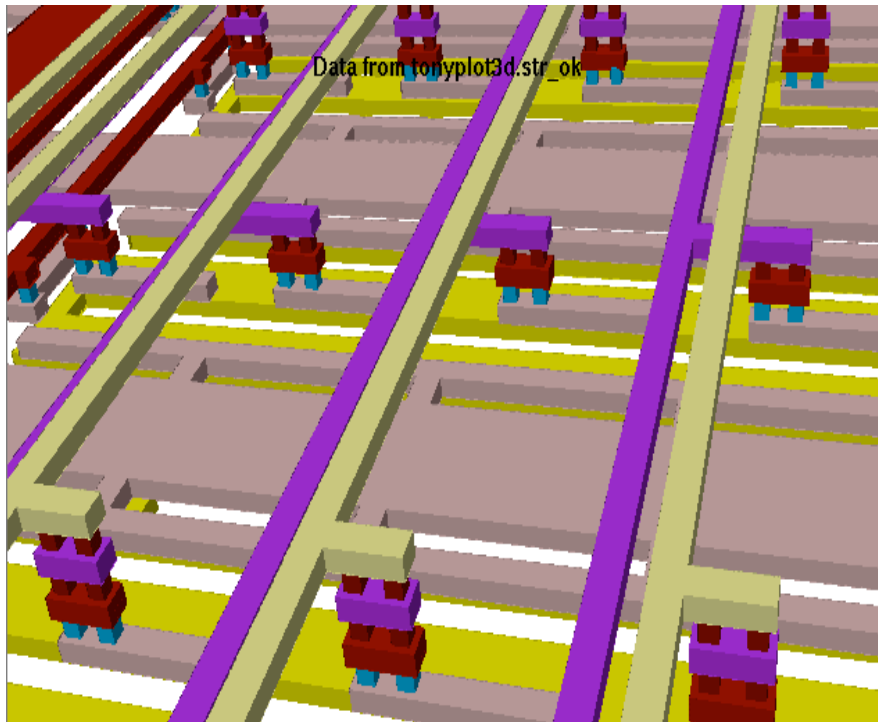
TonyPlot 3D: 3D Visualization Tool



Materials:	
aluminum4	Polysilicon
copper2	Copper
aluminum3	aluminum2
Aluminum	

Interconnect Modeling

TonyPlot3D: 3D Visualization Tool



Different views with or without meshing

Interconnect Modeling

Conclusion

- Very efficient extraction tool
 - Large cells
 - Fast
 - Ease of use of adoption
 - Direct Devices - Capacitances Netlist extraction
 - Unix, Linux available version