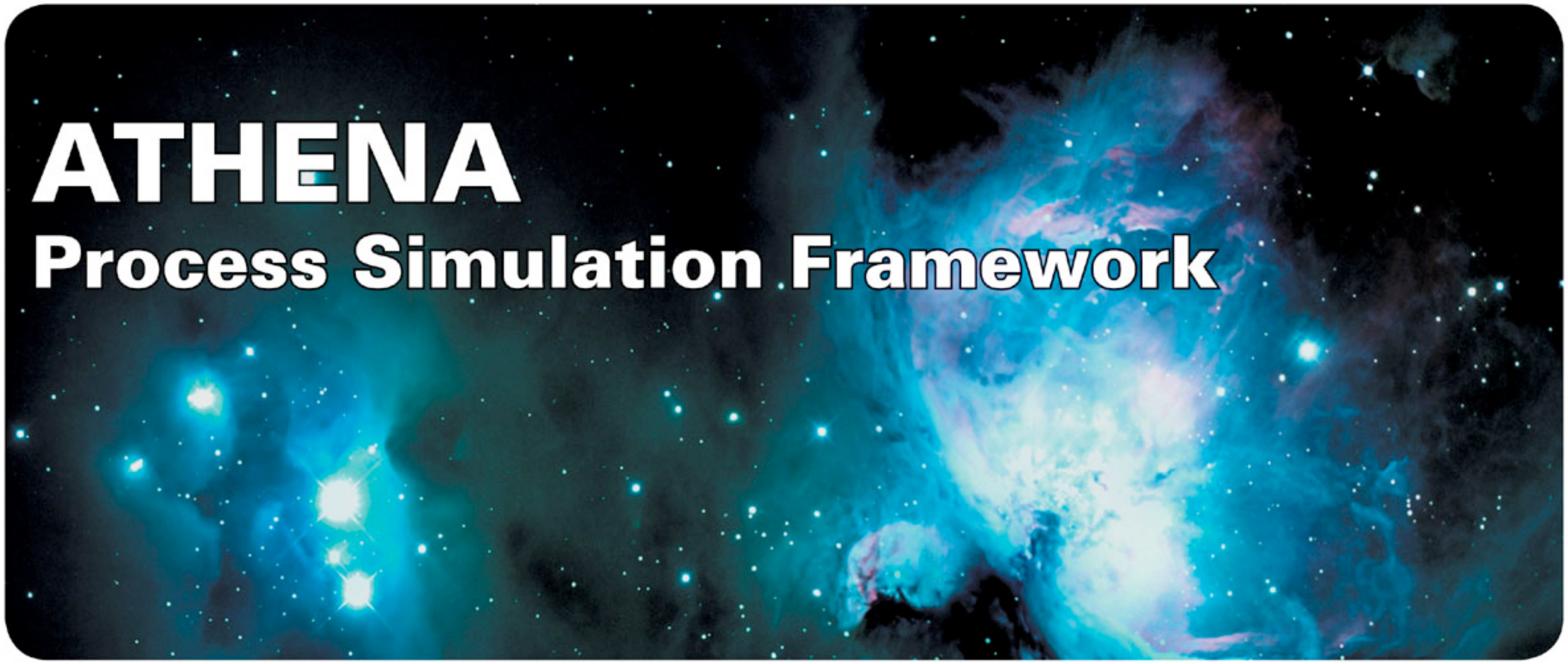
Backend Process Simulation Including Plasma Etch



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Introduction

- Elite as Part of ATHENA
- Processes Simulated by Elite
- Interaction of String and Gridding Algorithms
- Features of Elite include: Plasma Etching and Void Formation
- Step-by-Step Demonstration of Complex Trench Example

ELITE as Part of ATHENA

- ATHENA simulates all types of semiconductor technology processes
    - Inside wafer processes: Implant, diffusion, oxidation, defect generation, etc.
    - Topography processes: Deposition, Etching, Reflow, CMP, etc.
    - Photolithography processes: Imaging, Exposure, Photoresist Development
- In modern technologies these processes take place in any order
- Likewise ATHENA can simulate any sequence of processes

ELITE as Part of ATHENA (con’t)

- ATHENA invokes specific modules to simulate each process step
- In-wafer Processes are simulated by SSuprem4 or Flash Module
- Simple topography processes are also handled by SSuprem4
    - Geometrical or vertical etch
    - Conformal deposition

ELITE as Part of ATHENA (con't)

- Elite simulates more sophisticated deposition and etch processes
- Elite takes into account
  - Geometrical and rate characteristics of etch or deposition machine
  - Geometrical and material characteristics of the structure
- Photolithography is simulated by Optolith

Processes Simulated by Elite

- Topography processes are modeled by
  - Defining a machine in the `RATE.DEPO` or `RATE.ETCH` statement
  - Running the machine for a specified period of time
- Wet (Isotropic) Etching
  - WET and ISOTROPIC parameters in the `RATE.ETCH` statement
- Reactive Ion Etching (RIE)
  - RIE flag and combination of ISOTROPIC, DIRECTIONAL, CHEMICAL and DIVERGENCE parameters in the `RATE.ETCH` Statements

Processes Simulated by ELITE (con’t)

- Chemical Vapor Deposition (CVD)
  - CVD and STEP.COV parameters in the `RATE.DEPO` statement
- Deposition with different geometry of material sources
  - Unidirectional, Dual Directional, Hemispheric, Planetary, Conical
  - ANGLE1[ANGLE,ANGLE3], DEP.RATE, SIGMA.DEP parameters

Processes Simulated by ELITE (con’t)

- Monte Carlo Deposition
  - To estimate step coverage and film density
  - MONTE1/2, ANGLE, SIGMA.DEP, Sticking Coeff. parameters
- Chemical Mechanical Polishing (CMP)
  - Parameters in the `RATE.POLISH` statement
- REFLOW of glassy silica (oxide, BPSG,etc.)
  - Takes place simultaneously with impurity diffusion
  - When REFLOW flag set on the `DIFFUSE` and `MATERIAL` statements

Plasma Etching in Elite

- Monte Carlo based plasma etching model
- Calculates energy-angular distribution of ions emitted from the plasma of RIE etchers
- Etch rates in each point of complex topography are calculated
  - shadowing effects are take into account
  - etch rates could depend on local physical characteristics of the substrate (e.g. doping or stress level)

Plasma Etching in Elite (con't)

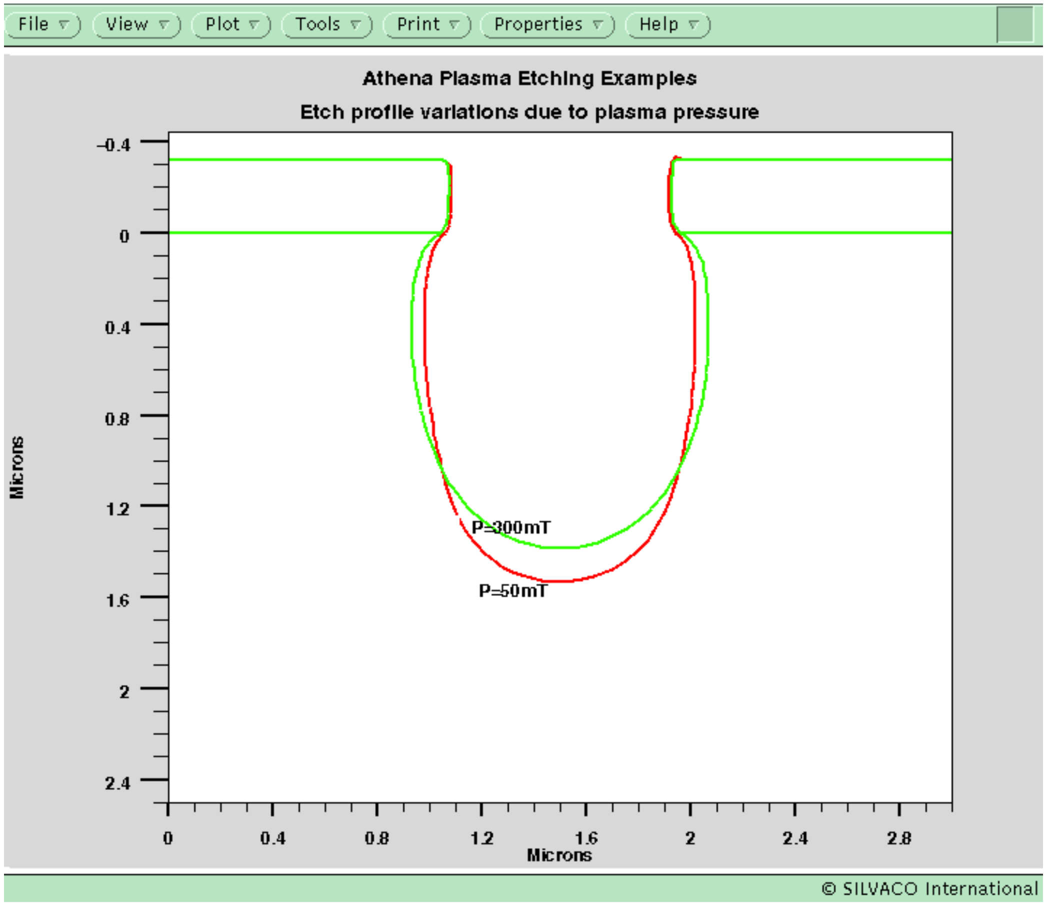
- Characteristics of plasma etching machine are specified as follows:

```
RATE.ETCH MACHINE=PETCH PLASMA \
  PRESSURE = 100 \    pressure                    [mTorr]
  TGAS = 300\         gas temperature             [K]
  VPDC = 32.5\        DC bias                     [V]
  VPAC = 32.5\        AC voltage in the sheath-
                      bulk interface              [V]
  LSHDC = 0.005\      mean sheath thickness       [mm]
  etc
```

- Relative etch rate coefficient for each material in the structure should be specified:

```
RATE.ETCH MACHINE=PETCH PLASMA MATERIAL=SILICON K.I=1.1
```

ATHENA Plasma Etching Examples – Etch profile Variations Due to Plasma Pressure



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Dopant/Stress Dependent Etching

- Dopant/stress dependent etching rate can be specified for any type of etching machine, e.g.:

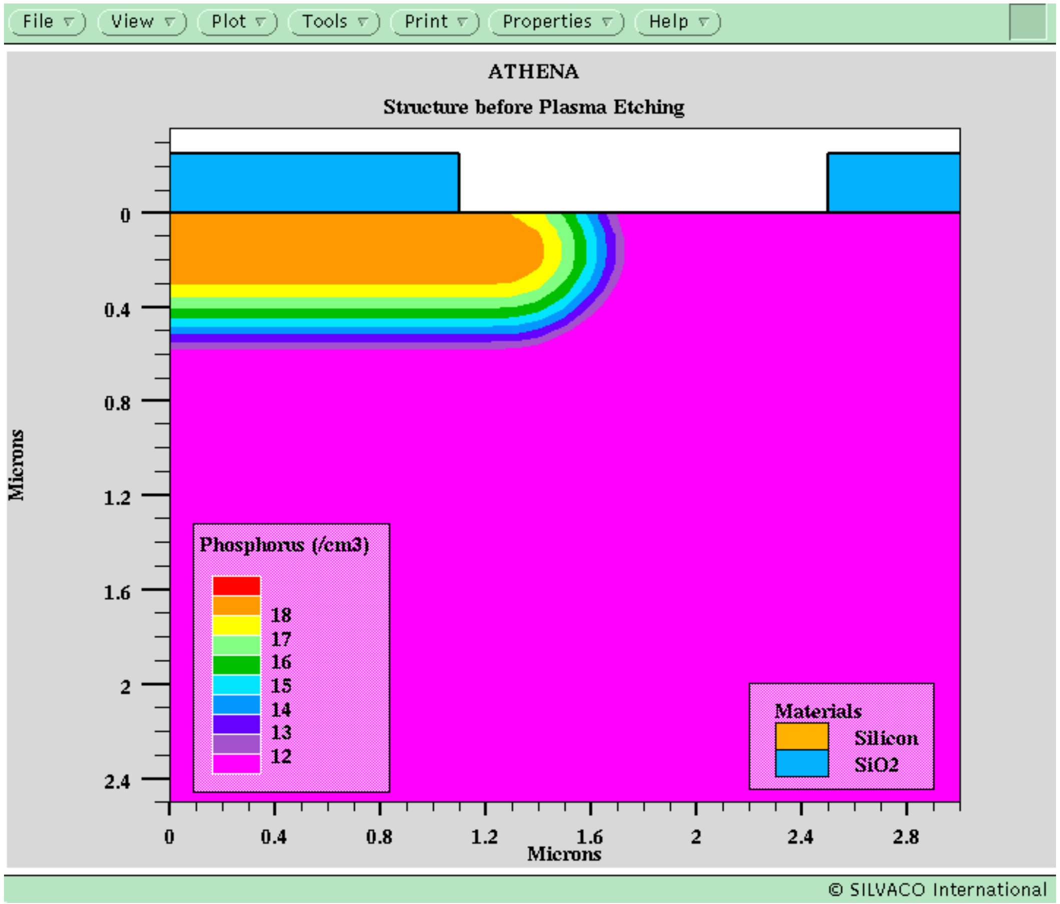
```
Rate.Depo Machine=RIE MATERIAL=SILICON\
  Impurity=Phos Enh.Max=2 Enh.Scale=5.0 Enh.minC=17
```

- The enhanced etching rate is defined by the equation:

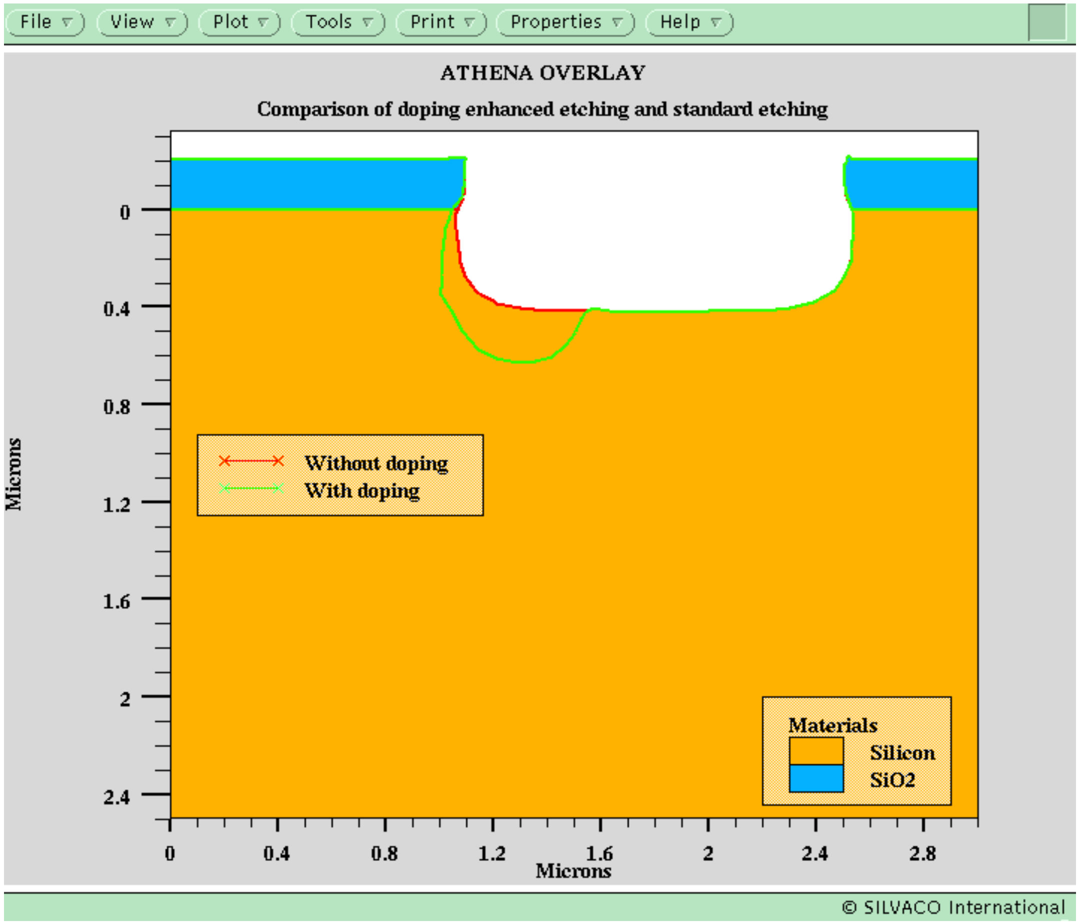
$$Er_{enh} = ER[1+0.5*Enh.Max\ (\tanh(Enh.Scale(C-Enh.MinC))+1)]$$

  - C is a solution (dopant concentration, stress, etc.)
  - Enh.Max defines the maximum enhancement factor
  - Enh.MinC is the value of concentration below which enhancement decays
  - Enh.Scale is enhancement scaling factor
  - For exponentially varying solutions both C and Enh.MinC are used in logarithimic form

Structure Before Plasma Etching



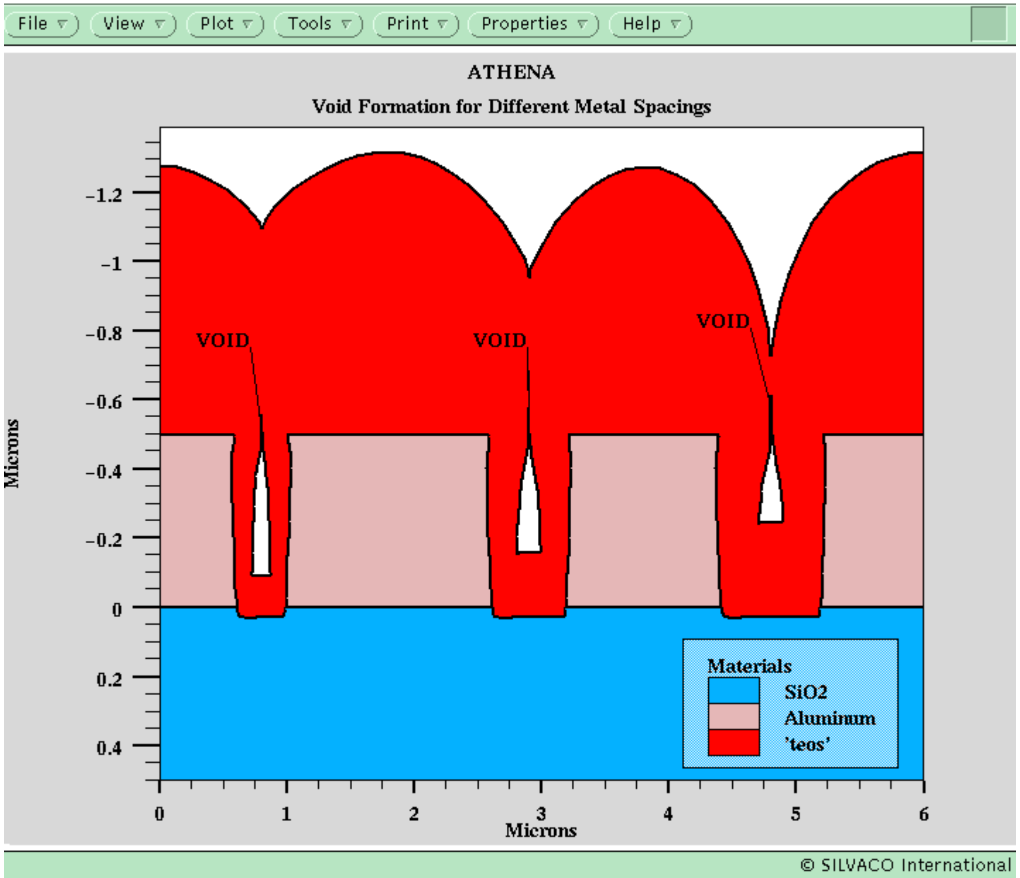
ATHENA Overlay – Comparison of Doping Enhanced Etching and Standard Etching



Void Formation in Elite

- Algorithm which allows formation of keyhole voids during material deposition into trenches or vias
- Void boundary condition are set correctly so subsequent deposits do not fill the void
- Void formation can be followed by simulation of viscous reflow of the deposited material to reduce or eliminate the void
- Next figure shows that the position of the void rises with contact width

Void Formation for Different Metal Spacings



Interaction of String and Gridding Algorithms

- In Elite, exposed surface is considered as a string of joined points
- During etching or deposition each point of the string advances
- New positions of each point are defined by local etch/deposition rate
- In contrast to other topography simulators, Elite links the string with a simulation grid

Interaction of String and Gridding Algorithms (con’t)

- During etching, the string cuts through into the grid
- Special regridding algorithm is applied to the area under the new surface
- During deposition, the string advances outside the simulation grid
- Special gridding algorithm is applied to cover newly deposited area

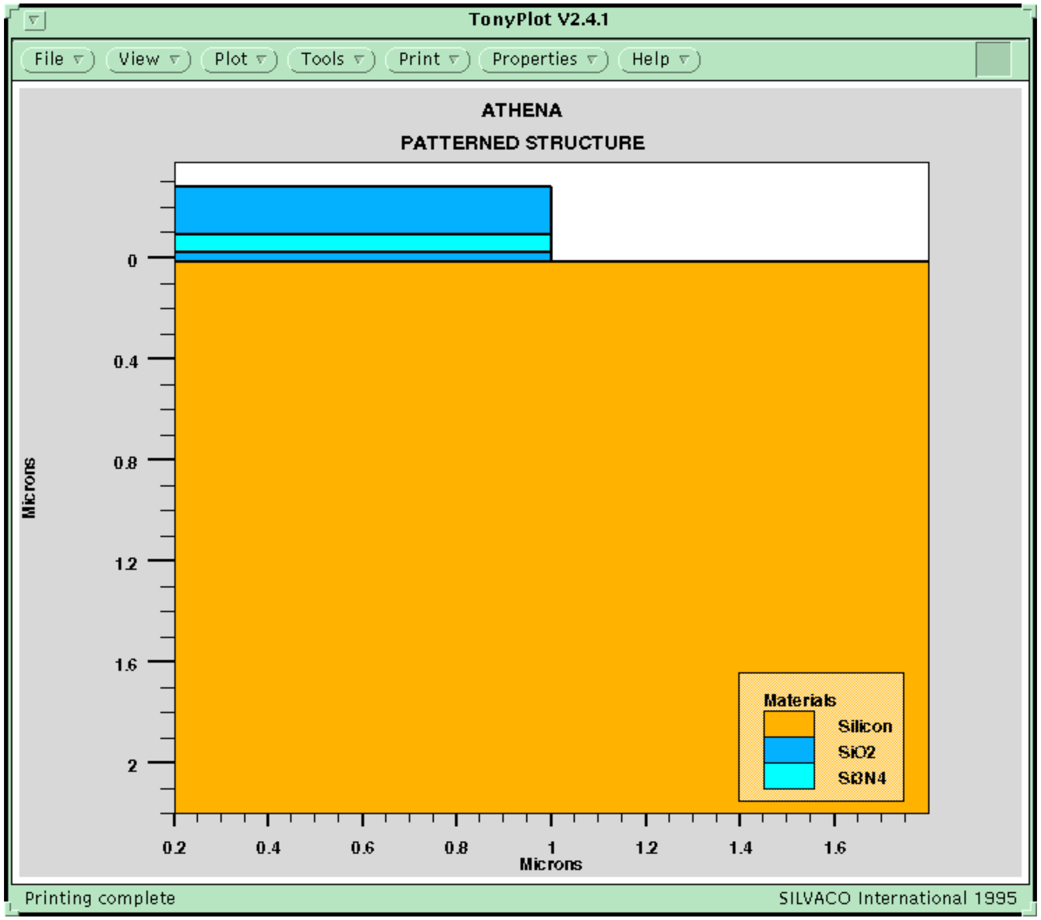
Complex Trench Formation Example

- Some of discussed Elite capabilities are demonstrated in the following example
- The example consists of a complex process sequence in order to show that ATHENA allows the easy transition from in-wafer to topography processes and back
- Demonstration is focused on Elite /SSuprem4 interface and on gridding issues

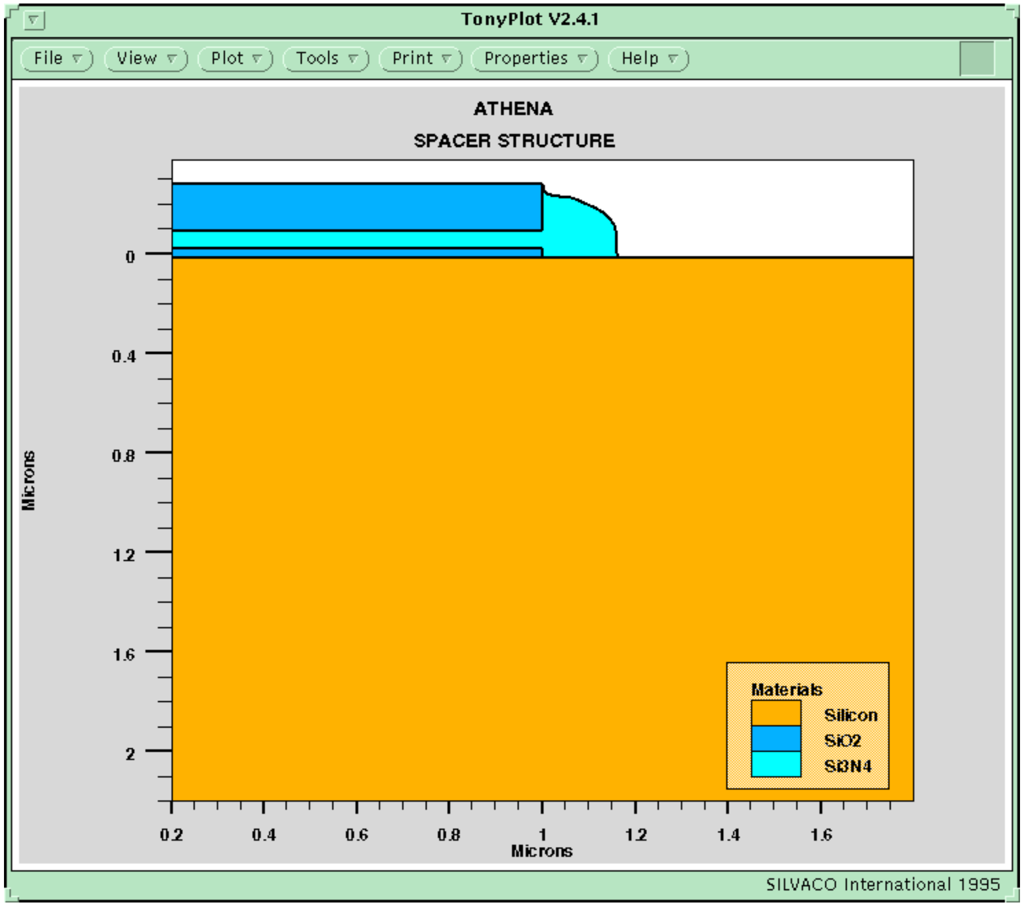
Complex Trench Formation Example (con't)

- First, an oxide/nitride/oxide stack is formed by oxidation and conformal deposition
- Then the stack is patterned using simplified mask process (Figure 5)
- After that a nitride spacer is formed by combination of conformal deposition and etch-back using RIE (Figure 6)
  - ISOTROP and DIRECT parameters are used to control shape and width of the spacer

Patterned Structure



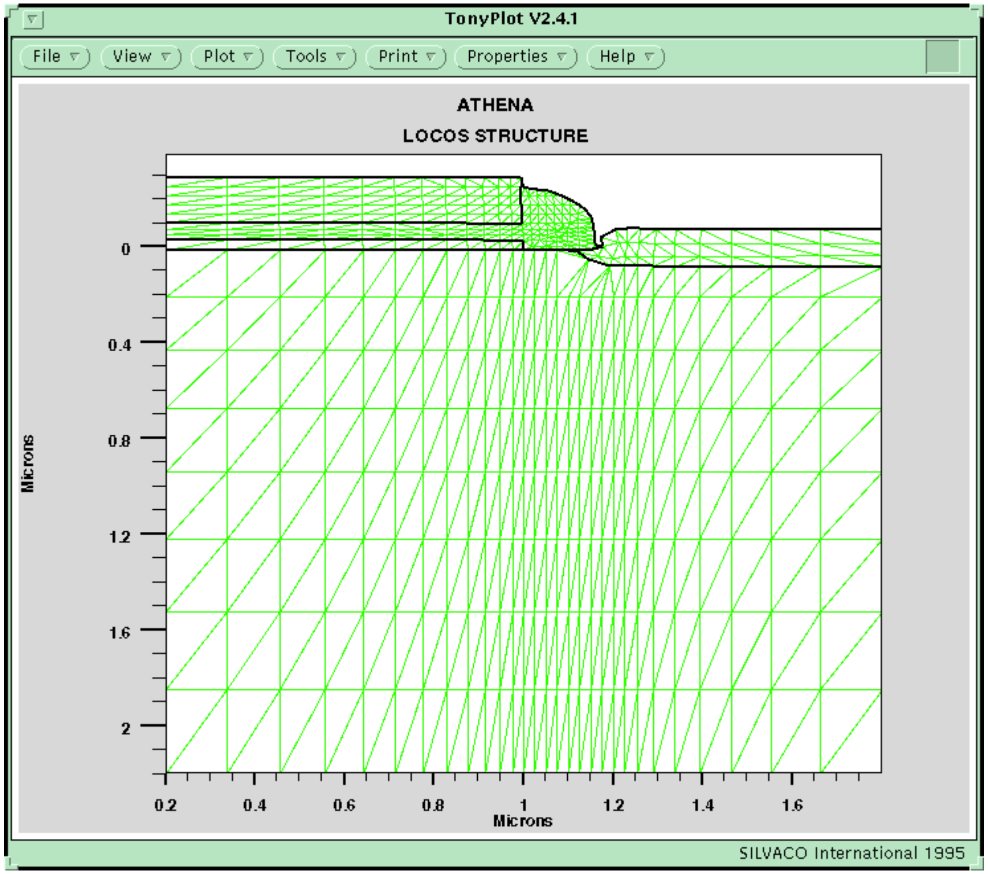
Spacer Structure



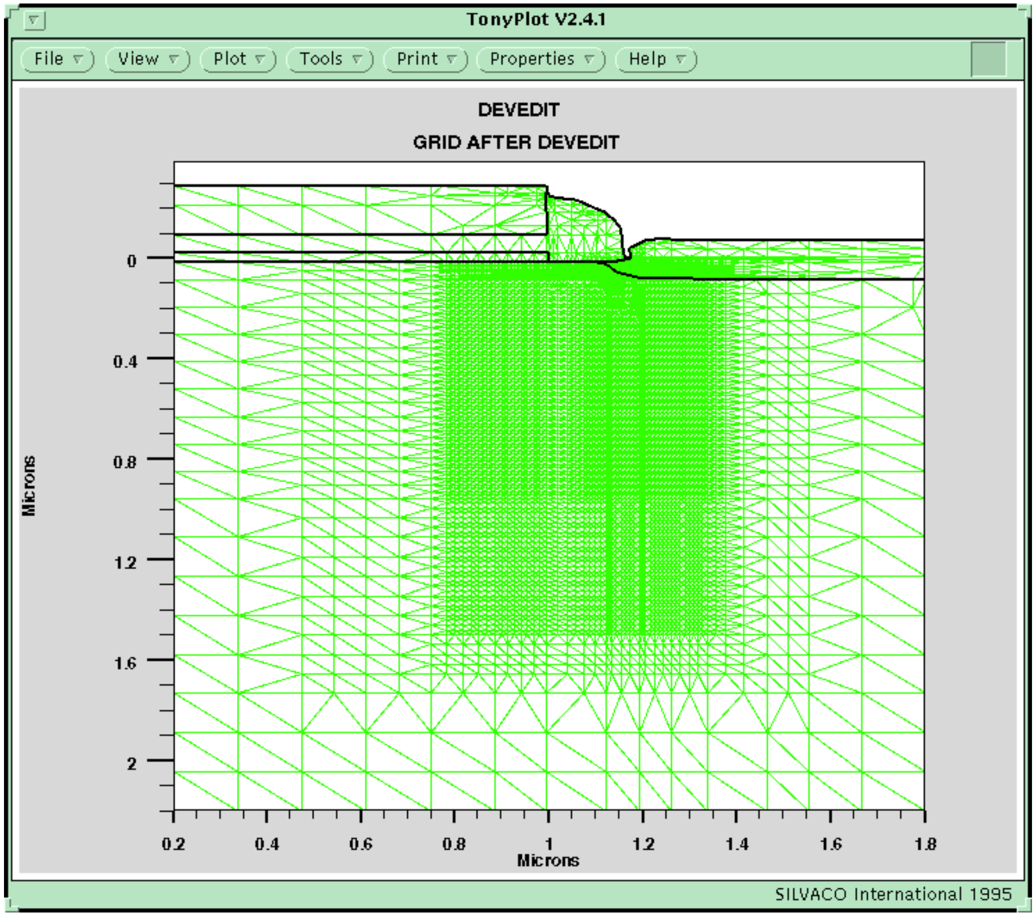
Complex Trench Formation Example (con’t)

- The thick spacer is used to reduce length of LOCOS with short Bird’s Beak
- Viscous stress-dependent oxidation gives accurate LOCOS (Figure 7)
- The grown LOCOS serves as a mask for subsequent Trench etching
- So far a very coarse grid in substrate was used. This saved a lot of simulation time
- Much finer grid is needed for trench formation and doping. This is achieved by DevEdit remeshing (Figure 8)

LOCOS Structure



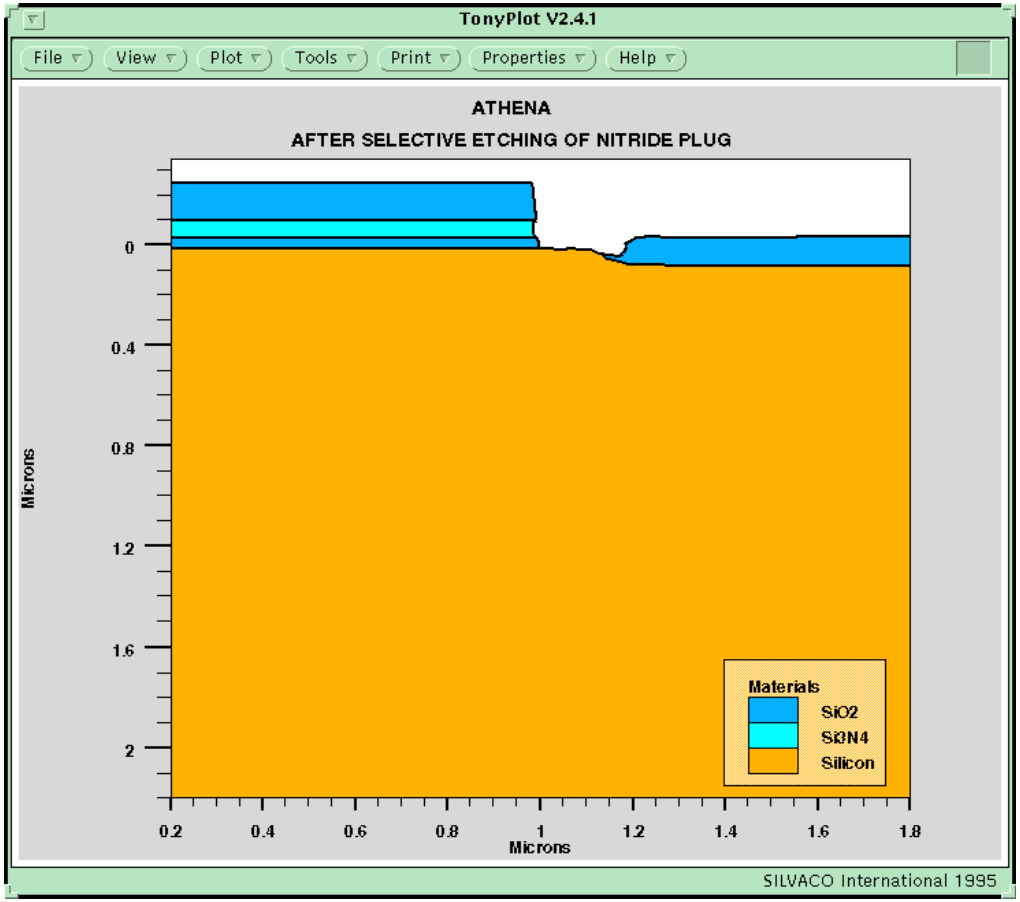
Grid After DevEdit



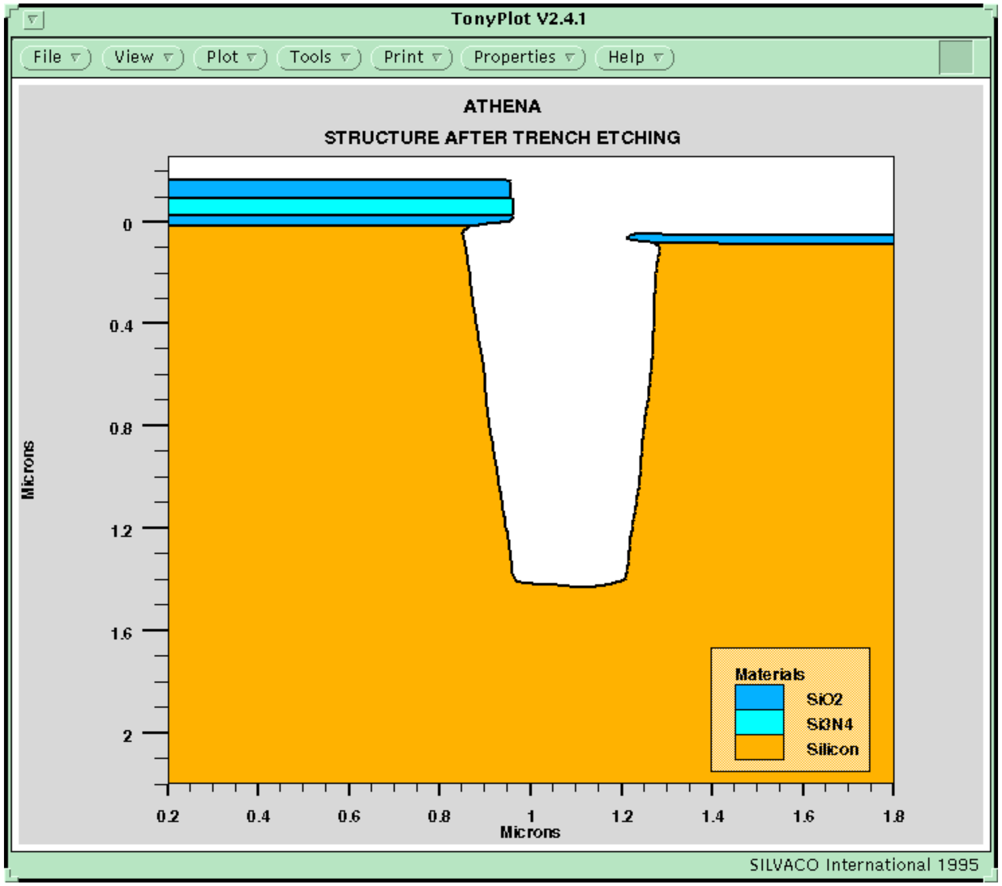
Complex Trench Formation Example (con’t)

- Next step opens a window for subsequent trench etching
- It uses a selective nitride etching simulated by RIE model with high directional etch rate for nitride (Figure 9)
- Deep trench is formed using high directional component of silicon etch rate (Figure 10)
- Tuning of the trench shape could be done by varying the isotropic rate

After Selective Etching of Nitride Plug



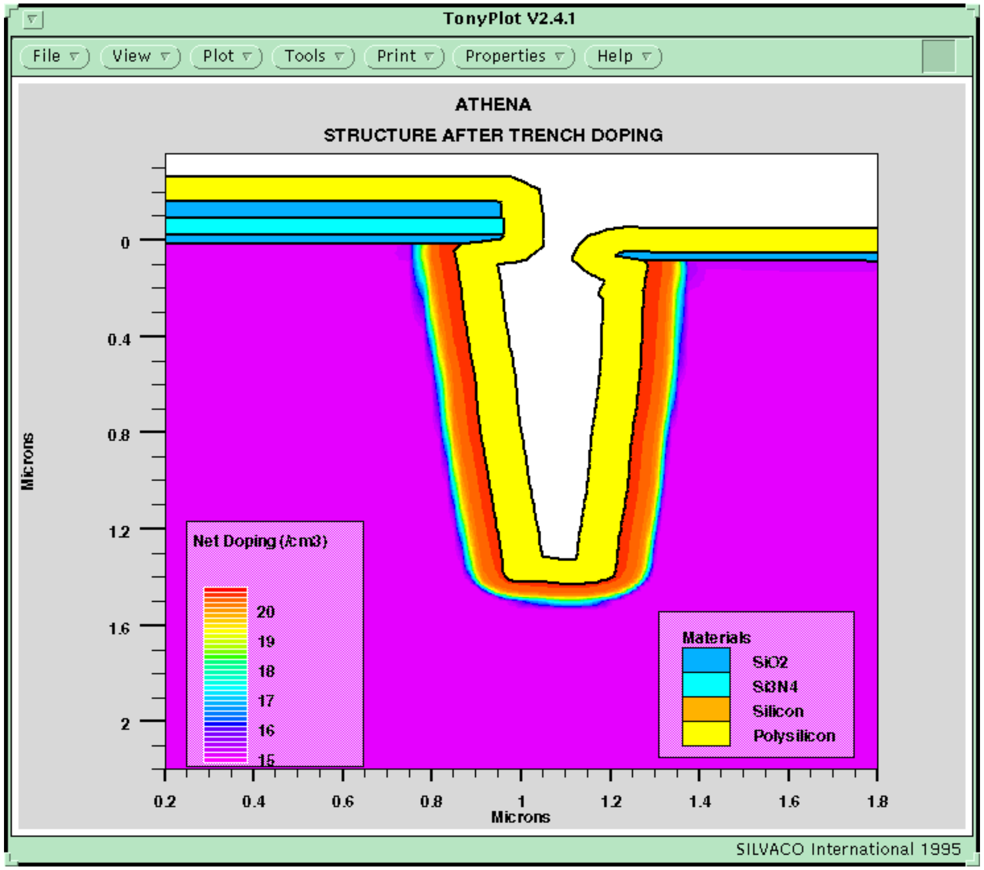
Structure After Trench Etching



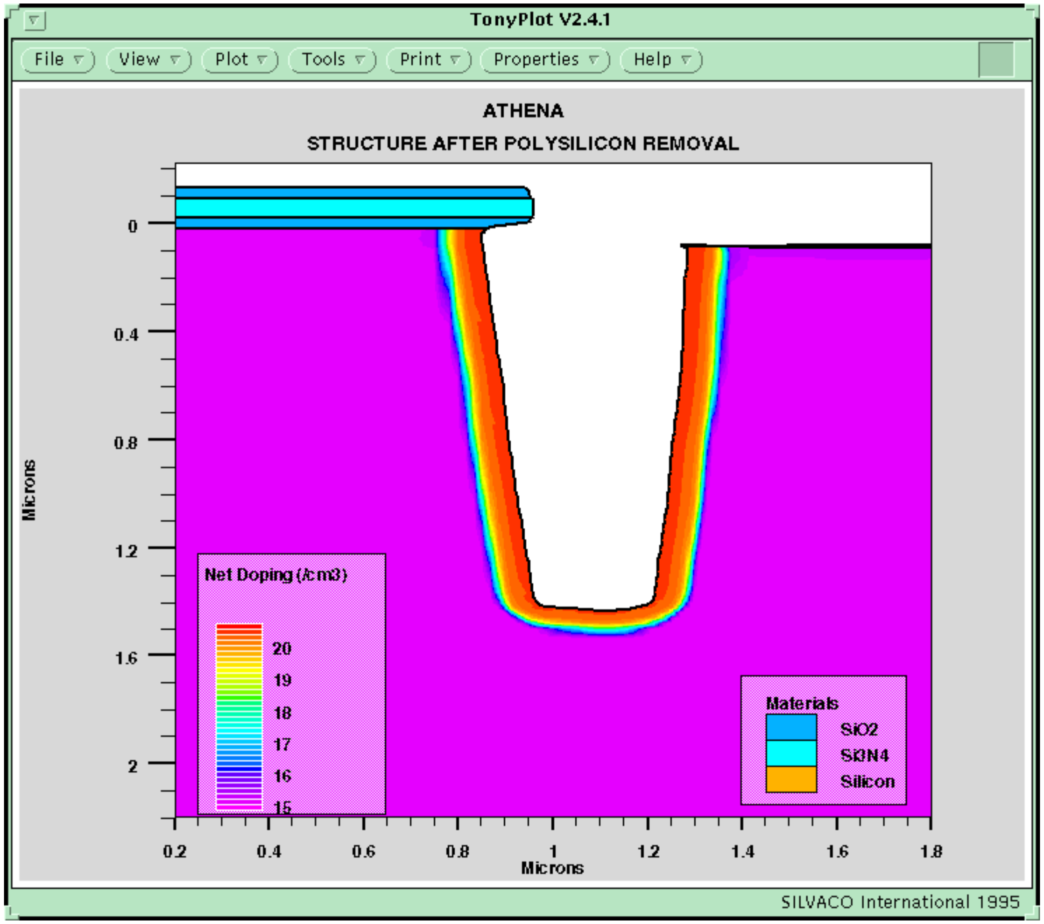
Complex Trench Formation Example (con't)

- Next step is to dope walls and bottom of the trench
- This is done by CVD deposition of phosphorus doped poly-layer and subsequent diffusion (Figure 11)
- It should be mentioned that substrate is not doped because thin oxide layer is left after trench etching
- Then polysilicon is etched completely (Figure 12)

Structure After Trench Doping



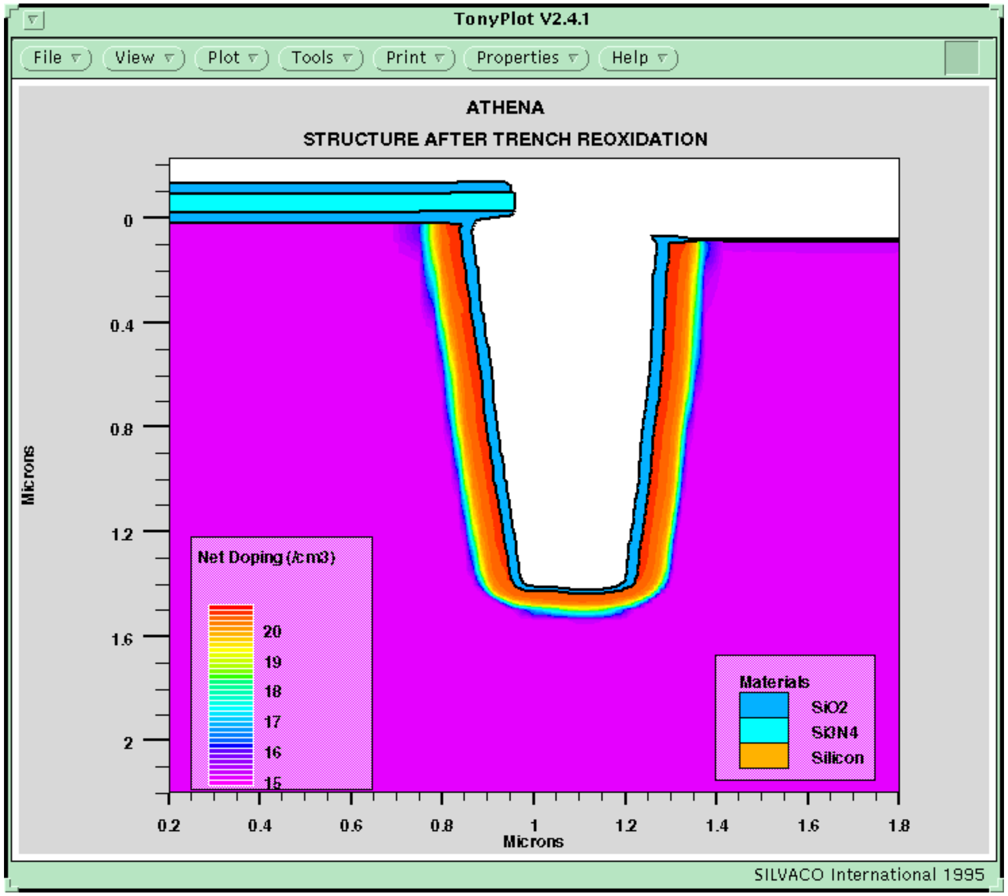
Structure After Polsilicon Removal



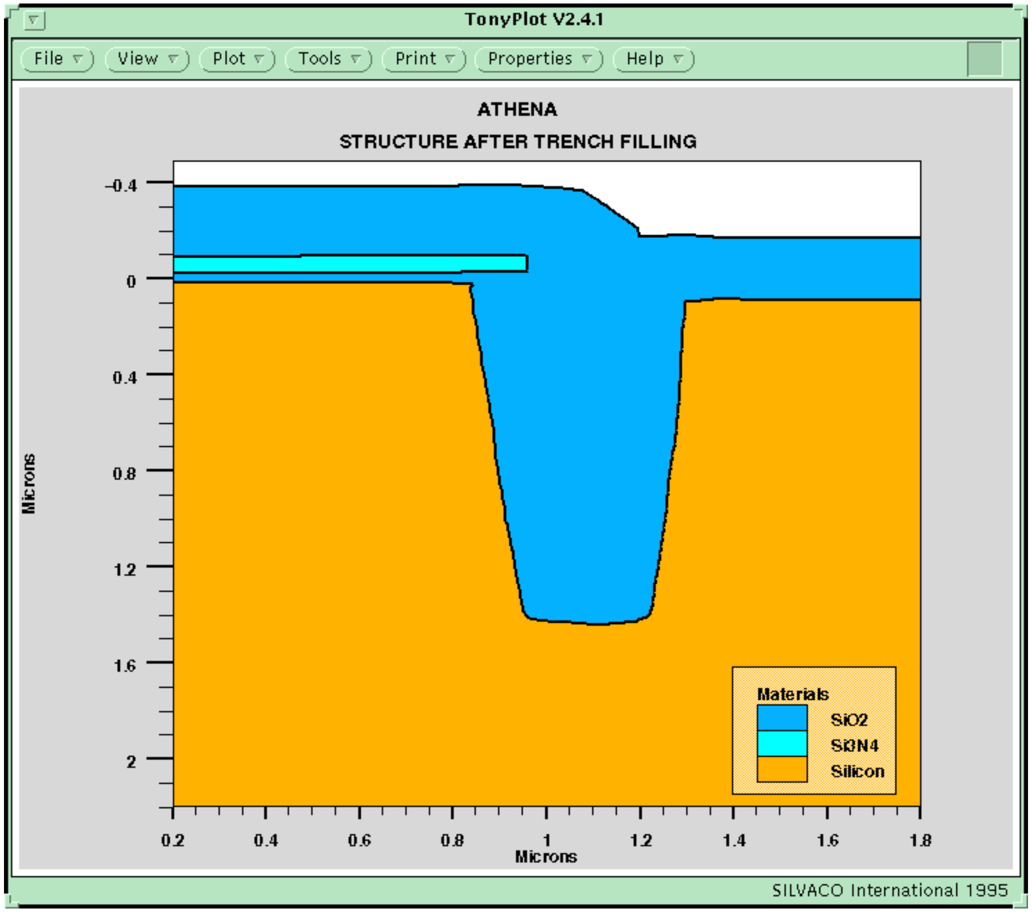
Complex Trench Formation Example (con’t)

- However, some residual polysilicon islands could remain after etching
- Slight reoxidation is used to consume these residuals (shown in figure on page 33)
- After that the trench is filled using oxide CVD deposition (shown in figure on page 34)
- A void could be formed in the process

Structure After Trench Reoxidation



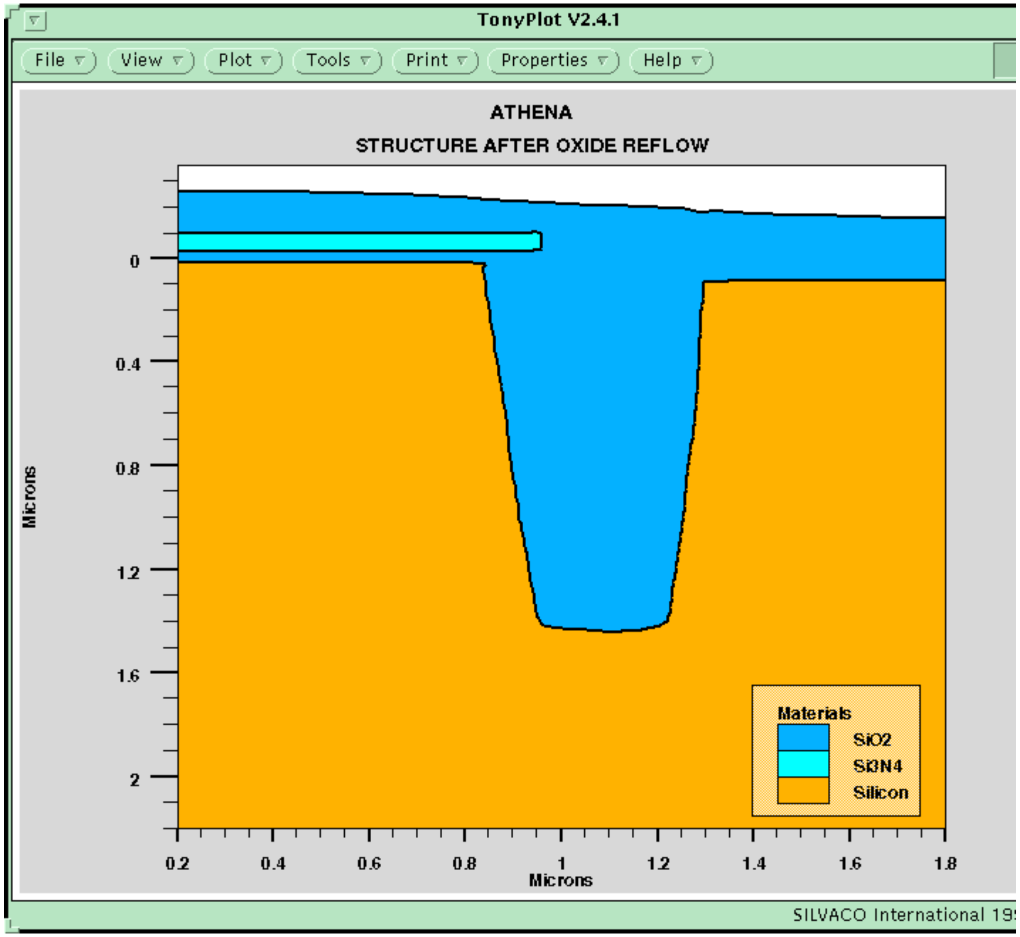
Structure After Trench Filling



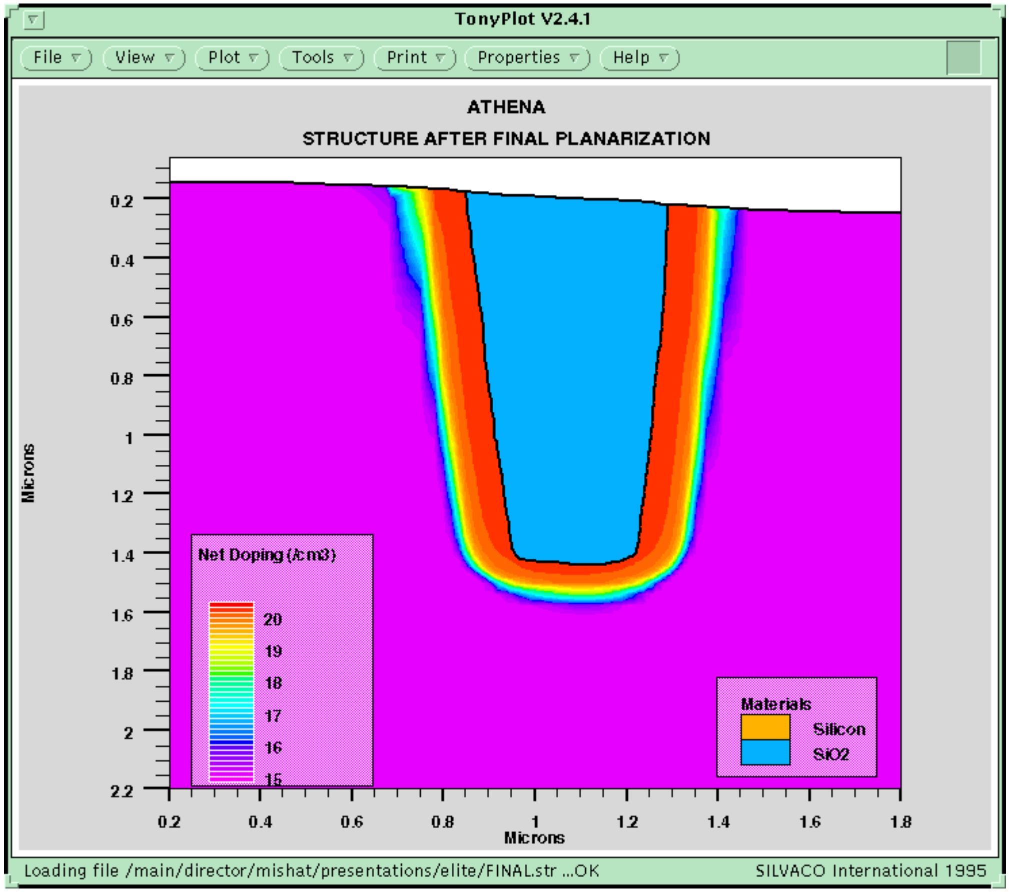
Complex Trench Formation Example (con't)

- After the trench is filled the outer oxide surface is always non-planar
- There are several methods of surface planarization
- One of them is viscous reflow which removes the step formed previously (Figure 15)
    - Impurity redistribution takes place simultaneously with reflow
- The final step of the process etches all excessive material layers and leaves only filled trench (Figure 16)

Structure After Oxide Reflow



Structure After Final Planarization



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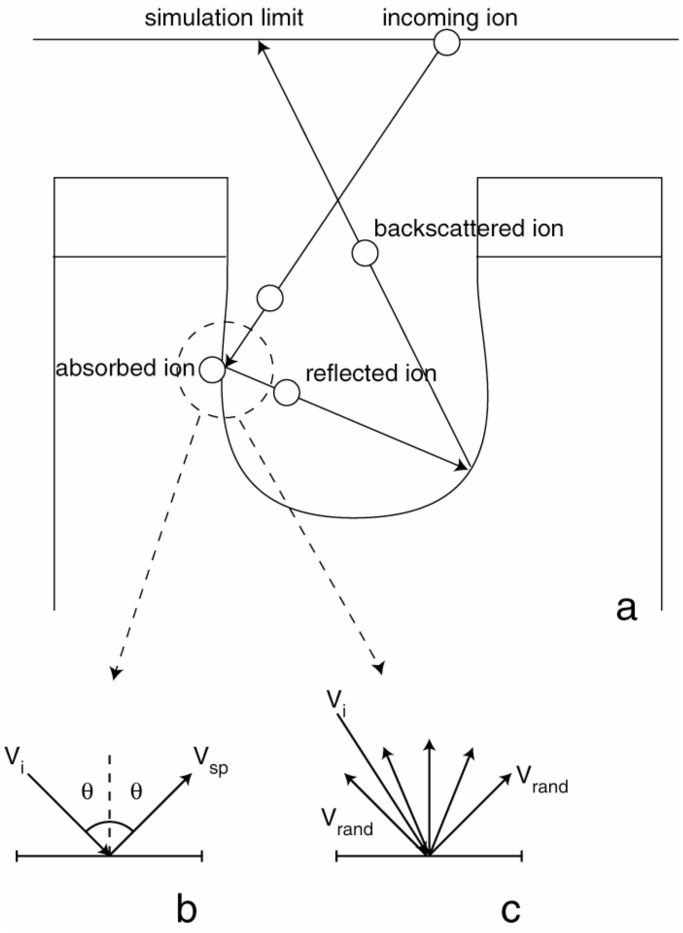
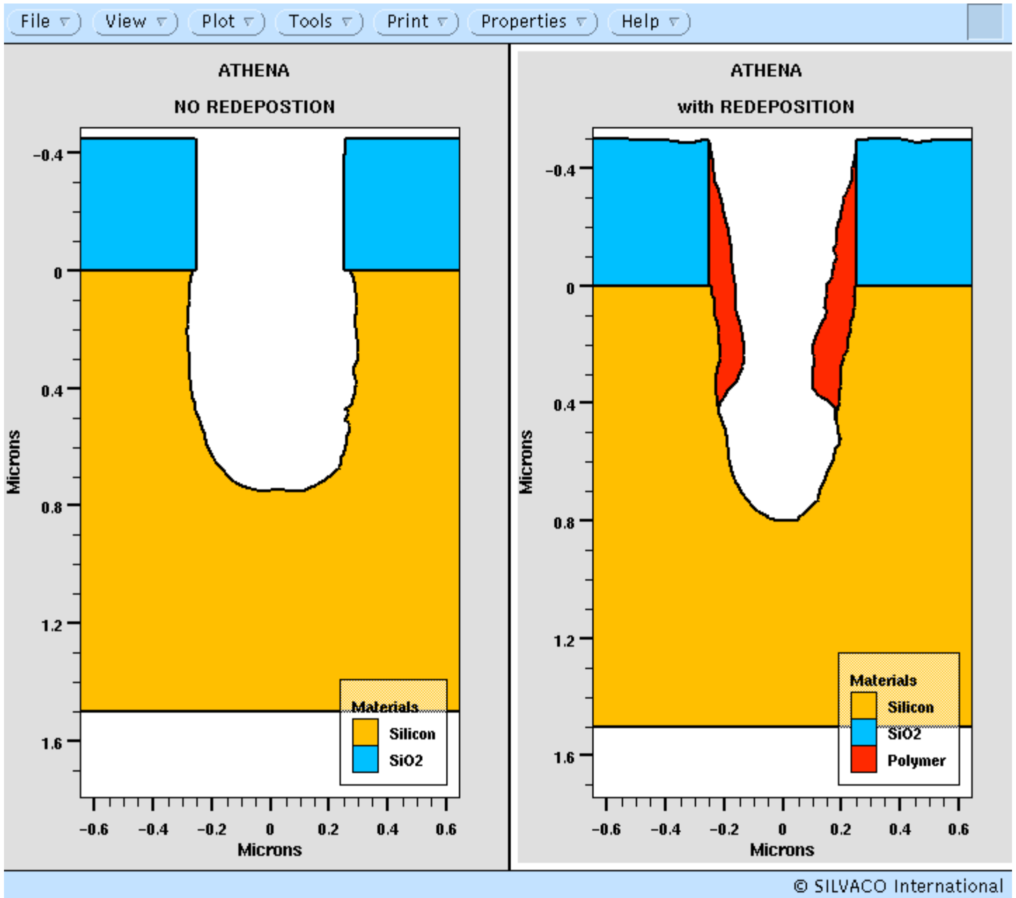
Schematic of Monte Carlo Etch



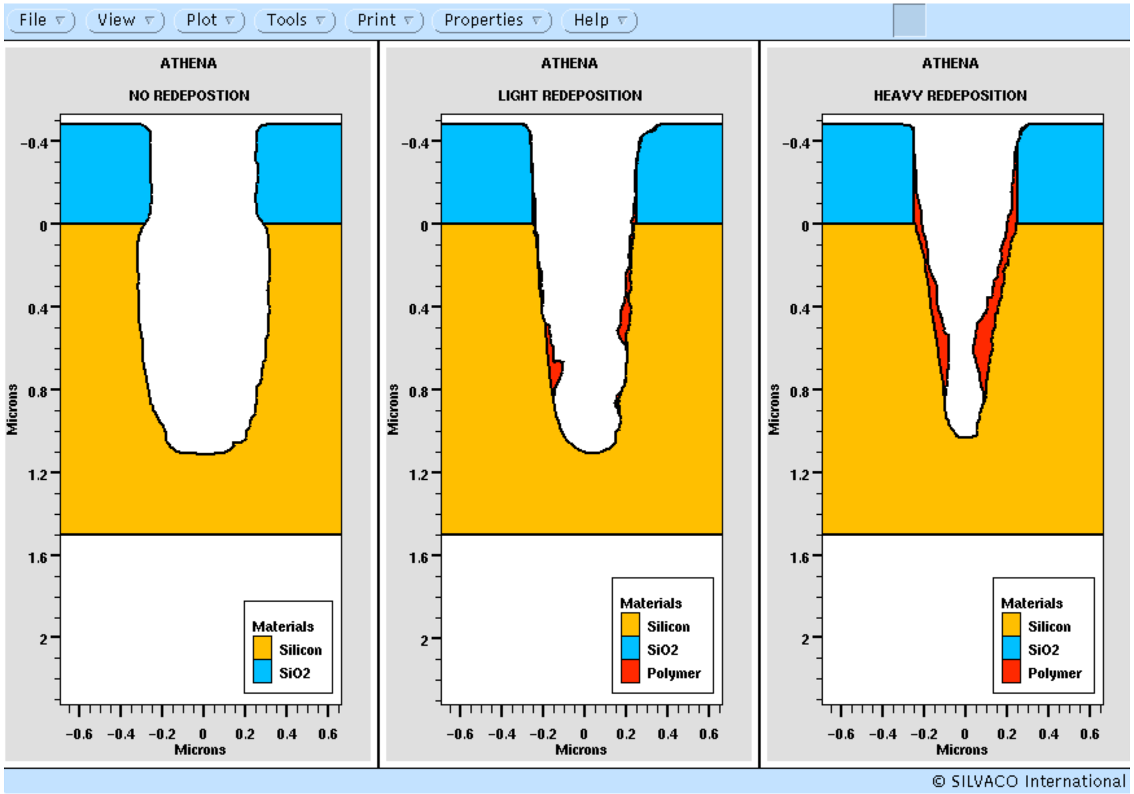
- Diagram of Plasma Flux algorithm (a) including zoom-in of ion reflection models (b and c)

Effect of Polymer Re-Deposition



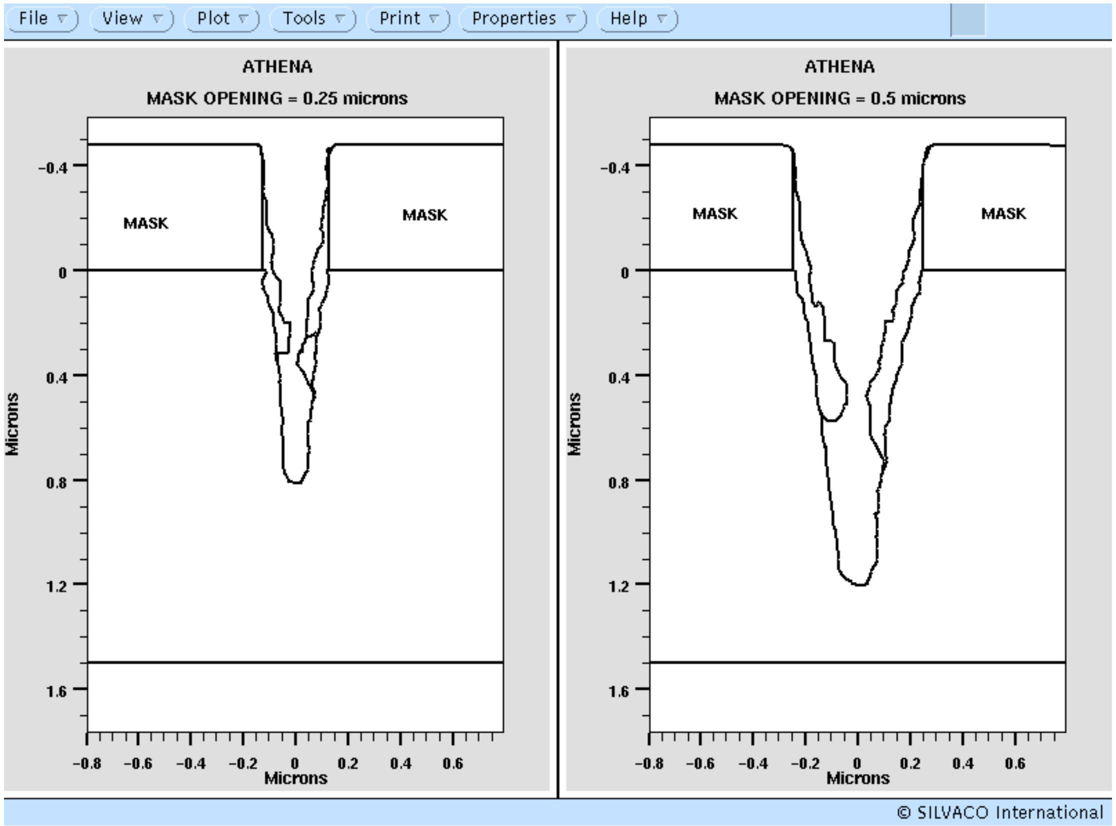
- Comparison of silicon trench etch with and without polymer redeposition

Deep Trench Etch Profiles



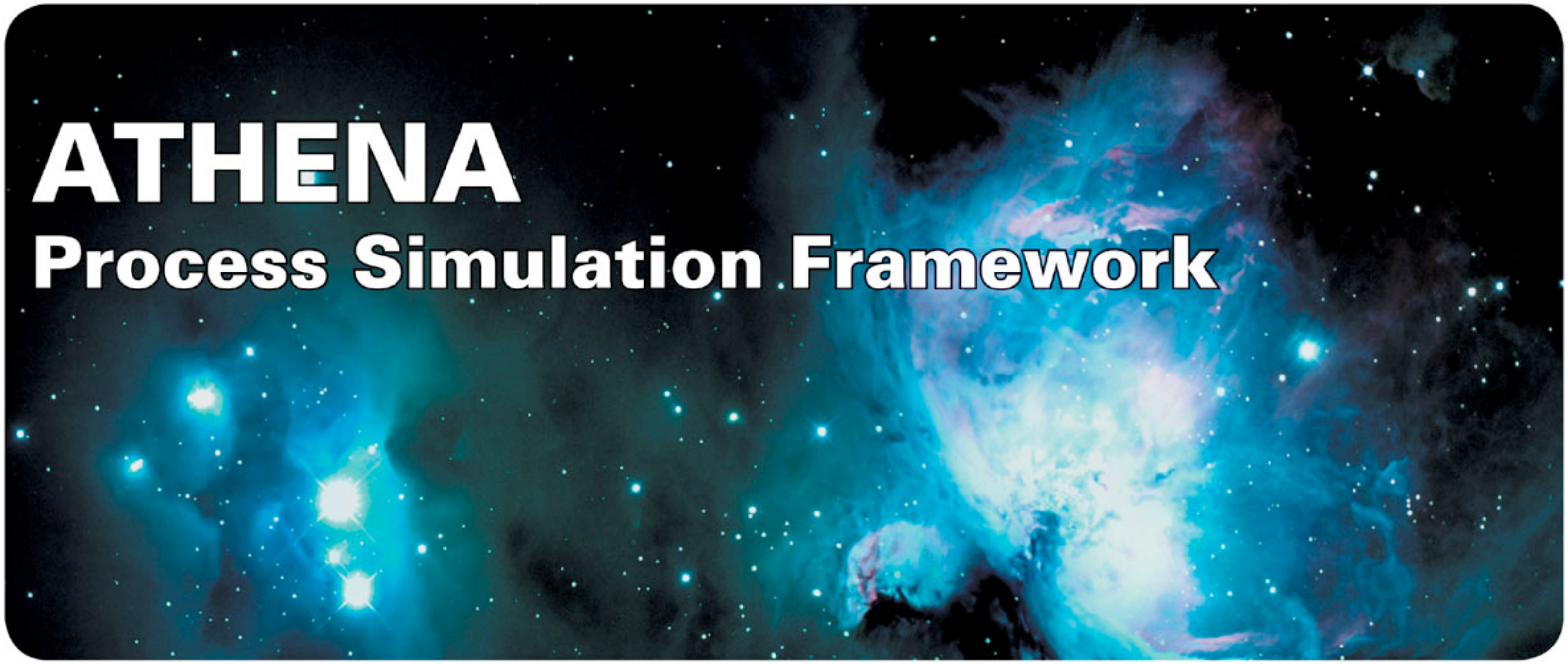
- Demonstration of the effect of redeposition on trench sideman Angle

Mask Opening



- Etch depth varies with the size of the mask opening as the redeposited material restricts etching the bottom of the trench

Chemical Mechanical Polishing in ATHENA



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Overview

- Effective planarization is an increasingly important process in any submicron VLSI device technology
- For five or more layer technology at least one layer should be perfectly planar
- Lack of planarity may cause serious problems for lithography and dry etching in sub 0.5 micron processes
- Increasingly popular planarization technique is CMP in which the wafer is held on a rotating carrier while its face is pressed against a polishing pad covered with a slurry of an abrasive material
- Allows very high degree of planarization because it is nonlocal process determined by the topography of the surrounding features
- Simulation of the process is very important due to its strong dependency on the device layout, pattern density, and topography from previous oxidations, etches, and depositions

Applications

- Emerged as a preferable planarization technique for several advanced technologies
- Main application is planarization of intermetal layer dielectric in multilayer interconnects
- has also been used to obtain high degree of planarity in submicron trench isolation process in MOS technology
- Similar techniques have been used for bipolar device isolation
- Such isolation techniques are extremely important when thermal constraints do not allow a more conventional LOCOS processing of silicon

Hard and Soft CMP Models

- Two different models (hard polishing and soft polishing) are implemented into ATHENA/ELITE
- Both models are phenomenological and based only on wafer topography
- They do not account for stresses of the polishing pad, fluid flow, removal of material by erosion, etc.
- The hard polishing model takes into account only nonplanarity of the wafer surface and adjusts the polish rate accordingly
- The soft polishing model accounts for flexibility and hardness of the polishing pad and reasonably defines the dependence of polish rate on the wafer shape

ATHENA/Elite Syntax

- The CMP module uses syntax similar to that of the etch simulation in Athena/Elite
- The **RATE.POLISH** statement is used to define the type of polishing to be used as well as the model parameters
- The hard and soft models could be used separately or simultaneously
- A small isotropic removal portion could be added using the **ISOTROPICAL** parameter which is usually much smaller than the lowest polishing rate
- The **POLISH** statement defines the time of polishing process as well as time and spatial discretization used in simulation

Hard Polishing Model

- This is a simplified version of a model by Burke (P.A. Burke, Proc. VMIC Conf. 1991, pp.379-384)
- The model uses a constant polish rate for areas above Ymax - dx and zero for areas below Ymax - dy. The rate is calculated from the pattern factor

  hardRate - max.hard * (1 - pf) + min.hard * pf)
- where : max.hard and min.hard are maximum and minimum polish rates specified in micron/sec, etc.
- pf is the pattern factor which is estimated as follows:

$$\frac{\text{pf = length of the surface (at Ymax - dy)}}{\text{total length of the surface}}$$

where: ymax is vertical position of current highest point; and dy is an average vertical shift during one time step

Soft Polishing Model

- Uses mathematical models of J. Warnock (J Electrochem. Soc. V. 138, pp. 2398 - 2402, 1991
- Models the pad flexibility (hard or soft) via the **LENGTH.FAC** parameter
- Models texture of the pad surface with the parameter **HEIGHT.FAC**
- Models erosion due to chemical slurry via the **KINETIC.FAC** parameter and and **ISOTROPICAL** component
- The **SOFT** rate and **ISOTROPICAL** rates can be set for each material

Conclusion

- ATHENA is based on a unified string/grid algorithm capable to simulate technology processes in structures consisting from many material regions of arbitrary geometry
- Combination of SSuprem4 and Elite within ATHENA framework allows to simulate complex process sequences which include both in-wafer and topography steps