Simulation and verification of void transfer patterning (VTP) technique for nm-scale features

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1. Introduction

The evolution of semiconductor devices into nano-regime has pushed researchers to look into nano-patterning techniques in order to understand the effects and properties at nanometer scales. Miniaturization based on optical lithography wavelength reduction has already hit a roadblock and the changeover to newer technologies is not financially viable for smaller manufacturers. The ability to create sub-lithographic nm-scale features without the need of high-end lithography tools will create new opportunities for the electronics industry. Thus, a reliable technique to form nanometer-sized structures is required for the realization of next generation nano-electronic devices. Some of the solutions for creating features below 180 nm include X-ray lithography [1], electron-beam (e-beam) lithography [2] and focused ion beam lithography [3]. However, these techniques lack in line-width homogeneity and suffer from lower throughput. Patterning of sub-lithographic features is still feasible and economical using other non-conventional techniques such as spacer patterning technique [4], resist ashing and trimming [5], electroplating [6] and lift-off process [7]. But, all these technologies are lithography dependent and inherit associated CD variations. This can be extremely crucial in memory applications where even subtle CD variations can affect vital device characteristics such as retention time and endurance.

The mainstay of this work is mathematical modeling, simulation and verification of a revolutionary void transfer process for patterning nm-scale features. This patterning process was originally envisioned by Breitwisch et al. [8] to demonstrate a fully integrated 256 kbit phase change memory (PCM) test array with 20–80 nm pore sizes using 180 nm CMOS technology. Sub-lithographic features are highly desirable in such devices in order to reduce the RESET/programming current of the PCM cells. However, most methods to produce sub-lithographic features inherit significant CD variation associated with the lithographic dimension. The void transfer process still requires a lithographically defined hole, but the combination of conformal deposition and accurate etch-back creates sub-lithographic CDs that are essentially independent of the original feature size. This ability to create nm-scale features opens a new era of collaboration for the realization of next generation bio- and nano-electronic devices. DNA and protein chips formed during void transfer process can potentially serve as fluidic channels for MEMS applications. Highly controlled nm-scale fluidic channels for use with MEMS applications is achievable due to the accuracy of controllability of LPCVD polysilicon process. Even
though the final pore size by this method is lithography independent, higher density of pores can be achieved as the lithography node shrinks. Thus, this process offers a simple technique for fabricating devices without the need of e-beam lithography and line-width beyond the scope of optical lithography. Finally, the ability to simulate these processes is extremely important because it enables faster technology development cycles by replacing expensive wafer fabrication processes with simulations and it provides information that is difficult or immeasurable.

Detailed topographical plasma simulations of reactive ion etching has been developed by Takagi et al. [11] by employing ‘Elite’ Monte Carlo etch module by Silvaco [12]. However, no simulation study of the void transfer process has been reported in the literature. In this study, simulation of void patterning technique for prediction of final feature size obtainable is investigated.

2. Process design

The void transfer process employed in this study is depicted in Fig. 1. As described in Ref. [8], the process essentially consists of: (1) deposition of a low stress thin film PECVD stack of SiN–SiO2–SiN-pad oxide on silicon wafers; (2) etching of a lithographically defined window of size ‘R’ (=2r) ceasing at bottom silicon nitride (SiN); (3) creation of overhang ‘A’ using selective isotropic etch in SiO2; (4) deposition of conformal LPCVD polysilicon that pinches off at top to deliberately form bottle shaped voids; (5) etching back polysilicon selectively to transfer the void to underlying SiN and (6) finally, removing the polysilicon stingers and SiO2 using a selective wet-etch leaving the small pores in SiN.

Fig. 2 defines the geometrical parameters as also described by Breitwisch et al. [8]. The critical parameters are: (1) the overhang ‘A’ must be less than ‘r’ for an effective CD miniaturization, and the void diameter depends largely on parameter ‘A’; (2) the thickness of SiO2 layer ‘T_SiO2’ must be greater than a certain minimum thickness ‘H_{min}’ in order to prevent the premature filling of lithographically defined holes without forming any voids and (3) sidewall angle ‘φ’ must be near 90° to get vertical profiles of final sub-lithographic pore instead of rounded sidewalls. The parameter ‘φ’ manifests from variation in angle ‘φ’ from 90° and leads in further reduction of void diameter ‘D’. The void size can be predicted using the geometry of the design.

From the triangle xyz in Fig. 2,

\[ H_{\text{min}} = r + \sqrt{\Delta^2 - r^2} \]  
\[ \Delta = r - \sqrt{T_{\text{SiO2}} (2r - T_{\text{SiO2}})} \]  
Where \( T_{\text{SiO2}} > H_{\text{min}} \) 

\[ \tan \theta = \frac{\sqrt{(\Delta - \delta)(2r - (\Delta - \delta))}}{\delta} \]  
\[ \text{Eq. (3) can be solved iteratively to get the value of } \theta \text{ that can be used to estimate the void size } D \]  
\[ D = 2(A - \delta) \]  

Table 1 gives the calculation results illustrating the effect of varying parameters on the final void size.

3. Experimental

A special test mask was made using Mentor Graphics mask layout editor and MEBES III electron-beam mask writer. It consisted of
different shaped features including lines for cross-sectional microscopy and density varying from 500 to 5000 nm and three different ‘R’ values of 500, 750 and 1000 nm. The maximum exposed area of the mask was kept lower than 25% to minimize the loading effects. Starting with 6° diameter (1 0 0) silicon substrates, a low stress thin film stack of SiN–SiO2–SiN with respective thicknesses of 150, 500–600 and 150 nm was deposited using plasma enhanced CVD in Applied Materials P-5000 system. Wafers were coated with FujiFilm OiR 620 M positive photoresist, exposed in a Canon i-line stepper and developed. The photoresist also served as an etch mask. It was observed that both the post-exposure and the post-development bakes caused resist reflow that led to mask faceting. As the unbaked resist withstood the subsequent stack etching, it was therefore not baked in this work. The top SiN was etched using SF6 + CHF3 chemistry in a Drytek Quad RIE tool followed by SiO2 etch using CF4 + CHF3 + O2 in Applied Materials P-5000 MERIE etch tool for a directional etch stopping at bottom SiN layer. Low temperature (550 °C) polysilicon was deposited in ASM LPCVD tool that was conformal causing pinching off at top to form voids. Void etch-back was done in Drytek Quad RIE tool with SF6 + CHF3 chemistry for directional etching and lower CD widening. A two-staged, CMOS compatible selective wet-etch process using buffered hydrofluoric acid and tetra-methyl ammonium hydroxide solution (TMAH) was developed to remove polysilicon stingers and the remaining PECVD SiO2. The process was characterized by examining the profiles using cross-sectional scanning electron microscopy (SEM).

4. Experimental results

With the trench aspect ratio of ~1, similar voids were observed in trenches of different densities. Fig. 3 shows an interesting SEM micrograph of a die region following the polysilicon etch. A stray contaminant particle is observed to have masked the etch leaving the original void intact that can be seen behind the etched void. Fig. 4(a) shows the cross-sectional SEM images of the voids with diameter of 74 nm when ‘R’ is 750 nm. Fig. 4(b–f) shows profiles at different stages of etch-back process. Fig. 4(g) shows the final sub-lithographic aperture in SiN with diameter of 130 nm which represents ~5.4 × reduction from the lithographic trench size ‘R’. Even though the diameter of transferred sub-lithographic aperture was higher than the void diameter, a higher aspect ratio trenches together with an accurately controlled deposition/etch-back process would promise lower CD widening to successfully pattern sub-100 nm features. Fig. 5 shows the statistical variation of pore sizes when parameter ‘R’ value of 500 nm was considered. The data was explored in the regions where deposition and etching were relatively uniform. In these regions, the minimum and maximum observed pore sizes were 184 and 237 nm with 11% standard deviation. In addition, the CD variation in this patterning technique has been reported by Breitwisch et al. [8] and Rajendran et al. [13] by electrically testing devices made in these sub-lithographic pores. The reduced spread in RESET current associated with CD variations in this process was observed when compared to spacer process [8]. Also, the lower dynamic resistance variability has been reported in the PCM devices made by the void transfer patterning technique when compared to devices made by conventional lithographic methods using resist trimming [13]. Furthermore, the degree of

![SEM micrograph showing a contaminant particle masking a portion of a die during void transfer etching.](image)

![X-SEM image of (a) void formed, (b–f) polysilicon etch-back and (g) final sub-lithographic aperture.](image)

![Statistical CD variation of the final pore sizes obtained in this work.](image)
the CD control in void transfer patterning technique greatly depends on the process controllability available from the tools used. Therefore this process will offer a much better CD control by using newer generation etch/deposition tools.

5. Process simulation

The process was simulated using various applicable model parameters of the Elite topography simulator module by Silvaco [12]. Elite is a topography simulator within ATHENA that consists of advanced 2-D Monte Carlo atomistic deposition/etch and plasma etching models in addition to primitive time based geometrical etching models. These models can be invoked by defining a machine that imitates experimental conditions in order to model the LPCVD and RIE processes. Process modifications can be implemented easily by altering individual machines without even affecting rest of the simulator. Elite is based on string algorithm that decides the topographical changes during the deposition and etching processes. It provides a set of etch models for different physical etching techniques. In order to conduct processing on a structure any model can be selected and invoked. The simulation physics involves the tracking of ion trajectories from the neutral plasma or bulk, through the dark sheath and walls by Monte Carlo method. The user-specified sheath thickness and the calculated mean free path length determines the collision frequency encountered by a particular ion. The final etch rate is estimated from the simulated Monte Carlo distributions that calculate an incident ion flux on the substrate surface and surface evolution is then displayed by string algorithm.

Fig. 6 shows the compiled simulation results for different density of initial lithographic holes. From the voids thus formed, it can be interpreted that density of lithographically defined holes does not affect the void formation as long as the LPCVD polysilicon is conformal. This is crucial for developing a high-density pattern transfer process that is scalable to future technology generations. For \( \alpha = 110 \text{ nm} \) and \( \theta = 80–89^\circ \), the diameter of void ‘D’ obtained from simulations was \( \sim 170 \text{ nm} \) which closely match with the predicted mathematical results as given in Table 1. The effect of variation in lithographically defined hole size ‘R’ (from 500 → 700 nm) is shown in Fig. 7(a). The values of ‘\( T_{SiO_2} \)’ and ‘\( \alpha \)’ were fixed at 600 and 100 nm, respectively which did not affect the void diameter if the critical conditions mentioned previously were still valid. However, it can be observed that if the hole diameter is increased but the ‘\( T_{SiO_2} \)’ kept same i.e. if the aspect ratios of trench is decreased, the voids are raised in height from the bottom SiN layer or in other words the void length ‘L’ is decreased. The raised voids are more prone to CD widening because of an inherent isotropic component during etch-back. Higher the isotropic etch component more is the CD widening. This effect is also observed experimentally as seen in Fig. 4, where the final sub-lithographic pore diameter is increased in size from void size of 74 nm due to smaller ‘\( L \)’ and raised voids. Therefore higher aspect ratios are desirable to yield more controlled pattern transfer with lower CD variations. Fig. 7(b) illustrates the results when the critical condition of ‘\( T_{SiO_2} > H_{Min} \)’ is intentionally violated resulting in premature filling of trench without any voids. Fig. 8 shows the effect of variation in ‘\( \theta \)’ on void formation. A deviation in sidewall angle from 90° results in sloping of voids that yields pores with sloped sidewalls. However, under controlled conditions this effect can be utilized to get even smaller features if pore slope is not that critical.

6. Simulation model calibration

The model parameters were explored to achieve a reasonable experimental correlation. The main parameters that control the
etch profile are pressure, ‘Vpdc’ (DC bias in plasma sheath), ‘Lshdc’ (mean sheath thickness), ‘Freq’ (frequency of current), ‘Mgas/Mion’ (the atomic mass of gas atoms and plasma ions), ‘Kf’ (plasma etch rate linear coefficient related to the ion flux) and ‘Ki’ (plasma etch rate linear coefficient related to the chemical flux). In order to simulate the effect of these parameters a calibration process was conducted in two stages as follows.

6.1. Stack trench etch and CVD model calibration

Fig. 9 displays the effect of parameters listed above on the etched trench profile and the void formation. It can be inferred from Fig 9(b) and (j) that neither the default model parameters nor the experimental parameters were sufficient to get a good agreement with the experimental results. Therefore extensive simulations were carried out. Row (1), Fig. 9 shows that varying ‘Ki’ and ‘Kf’ determine the sidewall angle of etched trenches. Parametric values were assigned to emulate the inherent ionic and isotropic etch components and the best settings are displayed in the last column of each row. Once these values were assigned, the effect of pressure was simulated and shown in row (2) of Fig. 9. Further fine-tuning the plasma sheath dc bias ‘Vpdc’, a successful correlation was achieved as observed from row (3). The polysilicon CVD process can be modeled by using conformal CVD model in ‘Elite’ by varying the step coverage factor in simulations. After calibrating different model parameters, excellent correlation with the experimental profiles was obtained as illustrated in Fig 9(i) and (k). Table 2 lists the model parameters and compares them with the experimental parameters.

<table>
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<tr>
<th>Ki</th>
<th>Kf</th>
<th>P</th>
<th>Mgas</th>
<th>Mion</th>
<th>Vpdc</th>
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<td>40</td>
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<td>200</td>
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</tbody>
</table>

Fig. 9. Simulation model calibration showing effects of variation in parameters on trench profile and void formation. Row (1) shows the effect of Ki and Kf, row (2) shows the effect of pressure, row (3) shows the effect of Vpdc and row (4) shows the profile obtained using experimental values and the experimental X-SEM image.

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agreement with the reported experimental values of keyhole size of 43 nm as illustrated in Fig. 10.

6.2. Void etch-back calibration

The void etch-back process was calibrated on similar lines to find the right parameter values also listed in Table 2. The experimentally observed profiles could be replicated by adjusting model parameters as shown in Fig 11. It was observed that the pressure adjustment (in 50–200 mTorr range) in the model had a relatively minor effect on etch profiles. However, the best match was observed using 200 mTorr in the model while the experimental value was 100 mTorr as given in Table 2. This is not surprising as the model may not exactly emulate tool/process specific conditions. Nevertheless it successfully models the process and offers a powerful simulator for the void transfer technique. The flowchart in Fig. 12 summarizes a methodology that could enable a unified simulation model coupling the geometrical and experimental process parameters.

7. Conclusions

In this study a robust yet simple void-assisted pattern transfer technique has been successfully modeled, simulated and validated. The results show that the 2-D Monte Carlo ion transport effectively simulates the plasma etching processes using standard dry etch chemistries used in this study. The critical factors influencing the void formation and pattern transfer have been identified. The void patterning technique can be potentially scaled to any technology node and can be modeled. This method provides a technique for creating nanometer scaled features for laboratories that are not equipped with the state of the art lithography tools yet are engaged in emerging device research requiring smaller dimensions. The simulation module demonstrated here will provide simulation capability for process development as well as a teaching tool.

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References