Power Device Physics Revealed

ATLAS
Device Simulation Framework

TCAD for Power Device Technologies
2D and 3D TCAD Simulation

SILVACO
Silvaco TCAD Background

- TCAD simulation leader since 1987
- Power device 2D TCAD simulation leader since 1992
- Power device 3D TCAD simulation leader since 1995
- Over 90% market share of TCAD-using companies
- Complete domination of TCAD university market share
- Recognized by customers as providing excellent, timely, worldwide local support
- Compatible with TMA and ISE legacy software for easy migration to SILVACO
Comprehensive TMA Compatibility

- SILVACO and TMA TCAD software share a common legacy from Stanford University
- ATHENA is T-Supreme4™ compatible
- ATLAS is MEDICI™ compatible
- This compatibility allows:
  - Direct loading of input deck syntax
  - Support for the same physical models
  - Use of the same legacy material parameters
  - Direct loading of TMA TIF format structure files
  - Sharing of users’ existing calibration coefficients

TMA Users can migrate to SILVACO software easily

T-Supreme4 and MEDICI are trademarks of Synopsys Inc
Objectives of this Presentation

- Presentation of simulation results for a wide range of power device types
- DC, AC, transient and breakdown voltage analysis
- Application examples:
  - SiC Trench Gated MOS Transistor
  - SiC DMOS Transistor
  - GaN Schottky Diode
  - GaN FET
  - Insulated Gate Bipolar Transistor
  - LDMOS, UMOS
  - Merged PiN Schottky Power Diode
  - Vertical Double-Diffusion MOS Transistor
  - Guard Ring
Application Examples

- SiC Trench Gated MOS Transistor
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Silvaco has developed and implemented extremely accurate Monte Carlo model for 3 SiC polytypes. The development was initiated by a SiC customer in Japan NJRC in 2003. Final doping profiles in SiC are extremely sensitive to IMPLANT ANGLE, and unlike other TCAD vendors Silvaco can accurately simulate this effect.
Doping Challenges for the SiC Technology

- Ion implantation is the only practical selective-area doping method because of extremely low impurity diffusivities in SiC.
- Due to directional complexity of 4H-SiC, 6H-SiC it is difficult ad-hoc to minimize or accurately predict channeling effects.
- SiC wafers miscut and optimizing initial implant conditions to avoid the long tails in the implanted profiles.
- Formation of deep box-like dopant profiles using multiple implant steps with different energies and doses.
Experimental (SIMS) and calculated (BCA simulation) profiles of 60 keV Al implantation into 4H-SiC at different doses (shown next to the profiles) for a) on-axis direction, b) direction tilted 17° of the normal in the (1-100) plane, i.e. channel [11-23], and c) a “random” direction - 9° tilt in the (1-100) plane (next slide.) Experimental data are taken from J. Wong-Leung, M. S. Janson, and B. G. Svensson, Journal of Applied Physics 93, 8914 (2003).
Experimental (SIMS) and calculated (BCA simulation) profiles of 60 keV Al implantation into 4H-SiC at different doses (shown next to the profiles) for c) a “random” direction - 9° tilt in the (1-100) plane ((a) and (b) shown on previous slide.) Experimental data are taken from J. Wong-Leung, M. S. Janson, and B. G. Svensson, Journal of Applied Physics 93, 8914 (2003).
Box profile obtained by multiple Al implantation into 6H-SiC at energies 180, 100 and 50 keV and doses 2.7 E15, 1.4E14 and 9E14 cm$^{-2}$ respectively. The accumulated dose is cm$^{-2}$. Experimental profile is taken from T. Kimoto, A. Itoh, H. Matsunami, T. Nakata, and M. Watanabe, Journal of Electronic Materials 25, 879 (1996).
Aluminum implants in 6H-SiC at 30, 90, 195, 500 and 1000 keV with doses of $3 \times 10^{13}$, $7.9 \times 10^{13}$, $3.8 \times 10^{14}$, $3 \times 10^{13}$ and $3 \times 10^{13}$ ions cm$^{-2}$ respectively. SIMS data is taken from S. Ahmed, C. J. Barbero, T. W. Sigmon, and J. W. Erickson, Journal of Applied Physics 77, 6194 (1995).
Channeling Dependant Phosphorous Implantation

Simulation of tilt angle dependence of Phosphorus ion implantation into 4H-SiC at 50 keV.
A typical 4H-SiC MESFET obtained by multiple P implants.

Multi-core computers significantly improve run times. This figure shows speedup achieved on 16 CPUs computer (Quad-Core AMD Opteron Processor 8356 x 4). The Well Proximity Effect was analyzed by running one million 300 keV Boron ion trajectories.

1 CPU: 6 h 40 min. vs 16 CPUs: 27 min.
Nitrogen Monte Carlo Implant into 4H-SiC Trench

- Tilted 20 degrees 25 keV Nitrogen implant into 4H-SiC trench. Simulation time for one million trajectories took 5 min.
Stress Simulation

The diagrams show stress effect formed during mask patterning after the RIE etching.

IV characteristics will be simulated taken into account the stress calculated in ATHENA.
Physical Models for SiC Device Simulation

- Quadruple Precision for wide bandgap material
  - Very low intrinsic carrier density
- Impurity-concentration-dependant mobility
- High-field-dependant mobility
- Interface state model (continuous TRAP in the band gap)
- Schottky contact (Parabolic field emission model)
- Self-heating effect
- Anisotropic model
  - Mobility
  - Impact ionization (0001, 112b0 for 4H-SiC)
  - Permittivity
  - Thermal conductivity
Impurity-concentration-dependant Mobility Model

Impurity-concentration-dependant Mobility Model

Impurity-concentration-dependant electron mobility and hole mobility of 1000-plane 4H-SiC

Impurity-concentration-dependant electron mobility and hole mobility of 1100-plane 4H-SiC
Field-dependant Mobility Model

Velocity-Field Characteristics for (0001) 6H-SiC for 23 C, 135 C, and 320 C, Simulated (solid lines), Experimental (symbols).

Velocity-Field Characteristics for (0001) 4H-SiC for Room Temperature and 320 C, Simulated (solid lines), Experimental (symbols)

Defect distribution

Fig. 1

Density of interface states extracted from n- and p-MOSCAPs using simultaneous high and low frequency capacitance-voltage measurements. The devices were annealed in NO for different times. The lines correspond to extrapolations used in the calculation of $N_E$. Reproduced from Ref. [5]

Ref) SiC & wide Gap Semiconductor Kenkyukai, p.15-16, 18th 2009

Definition of the continuous DEFECT distribution at the 4HSiC/SiO2 interface.
Anisotropic Mobility Model - Planar Type

- Structure and net doping
- Id-Vd curve

Isotropic mobility <1100>
Anisotropic mobility
Isotropic mobility <1000>
Anisotropic Mobility Model – Trench Type

Structure and net doping

Isotropic mobility <1100>

Anisotropic mobility

Isotropic mobility <1000>

Id-Vd curve
Temperature Dependence of Mobility

- The impedance is increasing as temperature is high due to the mobility model depend on the lattice temperature.

Id-Vd curve of SiC MOSFET for temperatures from -70 to 350°C.
Schottky Diode Leakage Current Simulation

- Quadruple precision simulation

![Graph showing Schottky diode leakage current simulation with and without field emission model.]

**4H-SiC**

1e16cm⁻³

Anode

Cathode

With Field Emission Model

Without Field Emission Model

Normal Precision

Quadratic Precision
pn Diode Breakdown Voltage Simulation

- Quadruple precision simulation

![Graph showing normalized and quadratic precision for a pn diode breakdown voltage simulation.](image)
4H-SiC Guard Ring Structure

No guard ring

With guard rings
Breakdown Voltage Simulation

Breakdown Voltage depend on the number of the Guard Rings

1D Planar

Same Vb on 6 & 7 GRs

Distribution voltage on each Guard Rings

Without GR

4H-SiC Guard Ring Breakdown Voltage depend on the number of Ring

Cathode Current (A)

GR01-1D.log
GR-Nashi.log
GR-1Ring.log
GR-2Ring.log
GR-3Ring.log
GR-4Ring.log
GR-5Ring.log
GR-6Ring.log
GR-7Ring.log
Breakdown Voltage Simulation

Impact Ionization + Current Flowlines

None

1 ring

2 rings

3 rings

4 rings

5 rings

6 rings

7 rings

Avalanche occur on the ideal position
MixedMode Simulation

- MixedMode

ATHENA Process Structure

ATLAS Simulation

IV Curve Set

Parameter Extraction

UTMOST

SPICE Model

Circuit Simulation

SmartSpice

ATLAS/MixedMode Simulation

Circuit Performance

SmartLib:
share with SmartSpice, UTMOST, ATLAS
MOS, BJT, TFT, Diode..
Active Device Models
MixedMode Simulation

- 2IGBT+Di(SiC)

![Diagram showing 2IGBT+Di(SiC) configuration with IGBT1, IGBT2, Di(SiC), L, R, Vdd, and Vgate connections.]

![Graph showing mixed mode simulation results with color coding for different layers and potential values in V.]
Application Examples

- SiC Trench Gated MOS Transistor
- SiC DMOS Transistor
- GaN Schottky Diode
- GaN FET
- Insulated Gate Bipolar Transistor
- LDMOS, UMOS
- Merged PiN Schottky Power Diode
- Guard Ring
Physical Models for GaN FET Simulation

- Automated calculation of Spontaneous and Piezo-Electric Polarization
- Automated calculation of Strain for the whole InAlGaN material system
- X and Y Composition Dependent Models for Bandgap, Electron Affinity, Permittivity, Density of State Masses, Recombination, Impact Ionization, Heat capacity, Refractive Index, low and high field Mobilities
- GaN specific Impact Ionization and Field / Temperature Dependent Mobility Models
- Phonon-assisted tunneling model
Schottky Diode Application Example – Reverse IV Characteristics

- Device Cross Section and Band Diagram of a n-GaN Schottky Diode

Schottky Diode Application Examples – Reverse IV Characteristics

- Reverse I-V Characteristic of a n-GaN Schottky Diode Showing Leakage Current due to Photon Assisted Tunneling versus Temperature

Schottky Diode Application Examples – Reverse IV Characteristics

Temperature dependence of Reverse-bias leakage current with and without Pipinis model

- $V_r = -20V$, $E = 85MV/m$
- $V_r = -10V$, $E = 46MV/m$
- $V_r = -4V$, $E = 31MV/m$

- $V_r = -26V$, $E = 65MV/m$
- $V_r = -10V$, $E = 26MV/m$
- $V_r = -4V$, $E = 31MV/m$
FET Application Examples – IV Characteristics

Id vs. Vgs characteristics suitable for $V_t$ extraction.

Id vs. Vds characteristics.
FET Application Examples – Optimizing Design

- Non Ideal Breakdown Characteristics using Standard Gate Field Plate Design. (Breaks down at 150 volts)
FET Application Examples – Optimizing Design

- After Optimizing Gate Field Plate Height and Over-Lap, a 600 volt breakdown was obtained.

A DOE can be created using ANY parameter in the input file since anything can be made a variable.
FET Application Examples – Self Heating Effects

- For GaN FETs on Sapphire or Silicon Carbide Substrates, Self Heating Effects are Significant. The slide below compares these effects on the resulting I-V and gm Curves.
FET Application Examples – Self Heating

- Comparing IdVd Curves for a GaN FET on Sapphire and Silicon Carbide Substrates respectively

![Graphs comparing IdVd curves on Sapphire and SiC Substrate](image-url)

Sapphire

SiC Substrate
Objectives of this Presentation

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Simulation of an IGBT

ATLAS Simulation of an Insulated Gate Bipolar Transistor

IGBT Net Doping

Collector Current vs. Collector Voltage

Drift (N-)

Sub (P+)

N+

P

IcVc Curve of IGBT

Collector Current vs. Collector Voltage

Log Collector Current (A/μm)

Collector Voltage (V)

Simulated Ic vs Vce Characteristics of the IGBT

Vg = 10V

Vg = 5V
Simulation of an IGBT

Lattice Temperature in the whole structure

This area has high electric field, so the lattice temperature increased

Emitter Region Lattice Temperature & Current Flow.
Simulation of an IGBT

- Curvetracer
  - Trace out complex IV curves (Latch-up, breakdown, snapback)
  - Dynamic Load Line Approach (Goosens et al., IEEE Trans CAD 1994, 13, pp. 310-317)

IBGT turn on as thyristor after the current reach to Latch-Up
Simulation of an IGBT

Current Flow During IGBT Latch-up

Collector Current and Lattice Temperature During Latch-up

The current flows after latch-up.
Simulation of an IGBT

- IGBT IcVce characteristics for temperatures from -70C to 300C

The impedance is increasing as temperature is high due to the mobility model depend on the lattice temperature.
Simulation of a 5000V IGBT Breakdown Voltage

- IGBT structure showing Electric field and potential distribution as well as impact ionization rate
Simulation of a 5000V IGBT breakdown voltage

- Breakdown simulation at different temperatures: 203K(-70°C), 300K(27°C) and 623K(350°C)

Breakdown Voltage and leak current depend on the lattice temperature
Breakdown simulation at different temperatures: 203K(-70C), 300K(27C) and 623K(350C)

Breakdown Voltage decreased due to the higher lattice temperature
Trench Type IGBT

- Comparison of Planar Type vs Trench Type IGBT
  - Comparison of Threshold Voltage, breakdown voltage and saturation voltage
  - Schematic Driven MixedMode for switching circuit performance analysis
IGBT Structures

- IGBT structure of Planar type (left) and Trench type (right)
Doping Profile of IGBT (Trench)

- 2D IGBT structure (left) and 1D (right)
- Doping profile along A – A’
Comparison of the Breakdown-voltage

- Breakdown curve of Planar type (Red) and Trench type (Green)
- Same Breakdown Voltage

Close Breakdown-voltage
Comparison of the Threshold-voltage

- Vge-Ic curves of Planar type (Red) and Trench type (Green) at Vce=10V
- Close Threshold Voltage
Comparison of the Saturation-voltage (VCE(sat))

- Vce-Ic curves of Planar type (Red) and Trench type (Green) at Vgs=15V

- VCE(sat) at Ic=10A/mm²
  Planar : 3.15V
  Trench : 2.35V
Switching Circuit Schematic with Inductor Load

> Switching circuit of Inductor for Fall-time measurement
> Gateway driven MixedMode simulation
> FWD (Free Wheel Diode) uses a Diode spice compact model
Comparison of Fall-time (Tf)

- Switching curves of Planar type (Red) and Trench type (Green) at 125°C.

- Tf: ② — ①
  
at IcP = 2.5A/mm²
  Planar: 510ns
  Trench: 470ns
Carrier Dependence on Switching Time (Trench)

- Distribution of Hole concentration during Switch-off

The tail current keeps flowing until the minority carrier (Hole) disappears
Figure of Merits

- Tf vs VCE(sat) trade-off curves of Planar type (Red) and Trench type (Green) at different carrier lifetimes

Trench type is Excellent

VCE(sat) [V] at Ic = 10A, Vge = 15V

Tf [ns] at Icp = 2.5A, Tj = 125°C

- tf, p = 1e-6s
- tf, p = 6e-7s
- tf, p = 2e-6s
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Simulation of a LDMOS Transistor

LDMOS Structure

Gate Charging Simulation
Simulation of a LDMOS Transistor

Cgg, Cgd @f=1MHz

ATLAS/S-FPICEC
Capacitance @ 1MHz Vdrain = 0V

Cgg

Cgd

Capacitance @ Vdrain=0V

ATLAS/S-FPICEC
Capacitance @ 1MHz Vdrain = 1V, 5V

Vdrain = 1V

Vdrain = 5V

Capacitance @ Vdrain=1,5V
3D Buffered Super Junction LDMOS

- 3D Process simulation done with VICTORY CELL showing Net Doping Distribution

Ref: IEEE circuits and Devices Magazine November/December 2006
3D Buffered Super Junction LDMOS

2D cutline through n-region.

2D cutline through p-region.
3D Buffered Super Junction LDMOS

Electric field distribution with 80 volts applied to the drain.

Impact ionization rate distribution at 80 volts drain voltage.
Super junctions are used in LDMOS to greatly increase the breakdown voltage of small geometry devices. This example illustrate the effectiveness of this approach for an electrical gate length of 2.5um the breakdown voltage is 85V.

Ref: IEEE circuits and Devices Magazine November/December 2006
The figure shows the UMOS device which has the Polysilicon gate in the form of the trench with rounded bottom. In order to perform accurate device simulation it is extremely important to have very fine conformal grid along the gate. The doping and grid around the bottom of the gate are shown in the insert.
Simulation of a UMOS Transistor
Merged PiN Schottky Power Diode

Net Doping Distribution

Electric Field distribution

Merged PiN Schottky Power Diode

Forward IV Characteristic

Reverse Breakdown Characteristic

Simulation of Guard Ring

Potential Distribution and Electric Field of the surface Guard Ring

Breakdown Voltage and the Potential of each Guard Ring
Summary

- SILVACO meets all key TCAD simulation challenges for all Power Device types in 2D and 3D
  - Need for wide temperature simulation range from -70°C to beyond 450°C
  - Need for simulation and extraction of very high breakdown voltages (600V, 1200V, 1700V, 5000V, 10000V) over wide temperature ranges
  - 2D and 3D stress simulation
  - 2D and 3D Monte Carlo ion implantation with special models for SiC for ALL implant angles