TCAD for Flat Panel Display
Silvaco Products – Connecting TCAD to Tapeout
FPD Design & Fabrication

EDA
- Verification
  - SPICE
  - Characterization
    - Parameter Extraction
    - I-V, C-V

Design house
- ECAD
  - System Design
  - Netlist Extraction
  - Circuit Design (Gateway)
  - Layout Extraction (HIPEX)

Front-End
- Layout Design (Expert)

Back-End

Manufacturing
- Mask
  - Recipe

Calibration
- TFT Process/Device
  - I-V, C-V

Verification

Characterization
- Process Simulation
  - LPE
  - DRC
  - I-V
  - C-V

TCAD
- ATHENA
- ATLAS

Analysis:
- Timing
- Power
- Noise
- Reliability

EXACT
- CLEVER
- STELLAR

Silvaco
Silvaco Solution for FPD applications
ATHENA – Process Simulation
  ▪ ATHENA modules
ATLAS – 2D/3D TFT Device Simulation
  ▪ Pisces/TFT
  ▪ a-Si/poly-Si TFT device models & simulation examples
  ▪ MixedMode – TFT device + Spice circuit
  ▪ OTFT/OLED – Organic Devices Simulation
Clever - 3D Field Solver for Parasitic RC Extraction
  ▪ AMLCD Pixel RC Extraction: Spice netlist extraction
  ▪ LC Modeling: Verilog-A
UTMOST – Spice Parameters Extraction & Modeling
SmartSpice - Analog Circuit Simulator
Silvaco Solution for FPD Applications

- LCD TFT
  - a-Si TFT-LCD: low price, improved performance
  - Low temperature Poly-Si TFT-LCD: System On Panel
  - CG Silicon TFT-LCD: LSI + LCD

- Organic EL Display
  - Large Scale, micro scale _ TFT New Age
    - Large circuit, multi-layer interconnection
  - Stability & Reliability, Organic EL material

< Silvaco Solution >
- TFT/Organic Device: ATHENA/ATLAS
- Interconnect Parasitic RC: CLEVER
- Circuit: SmartSpice64
Silvaco Solution for FPD Applications
ATHENA – Process Simulation

- **SSuprem4 Models**
  - Ion Doping (Implantation)
    - SVDP (Sims Verified Dual Pearson)
  - Diffusion
    - Dopant & Defects Fully coupled Diffusion Model
    - Polysilicon Diffusion Model in Grain/Grain Boundary
    - PLS – New Advanced Diffusion Model in Silicon
  - Etching/Deposition – Conformal Geometry
  - Silicide

- **MC Implant – Monte Carlo Ion Implant**

- **Elite**
  - Advanced Etching/Deposition – Complicated Topography
  - Polymer Redeposition – Plasma Etch

- **Optolith – Optical Lithography Simulator**
TFT-LCD Simulation

Pixel Structure and TFT Device for Simulation
TFT Process Simulation Using SSuprem4
TFT Process Simulation Using SSUPREM4: TFT Structure Generation
ATLAS – 2D/3D TFT Devices Simulation

- Pisces/TFT
- a-Si/poly-Si TFT device models & simulation examples
- MixedMode – TFT device + Spice circuit
- OTFT/OLED – Organic Devices Simulation
Pisces/TFT

Drift-Diffusion model – Poisson + Current Continuity Eqs.

\[
\text{div}(\varepsilon \nabla \psi) = q \left( n - p - N_D^+ + N_A^- \right) + Q_T
\]

\[Q_T = q (p_t - n_t)\]

\[n_t = \text{DENSITY} \times F_n\]

\[p_t = \text{DENSITY} \times F_p\]

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \text{div} \vec{J}_n + G_n - R_n
\]

\[
\frac{\partial p}{\partial t} = \frac{1}{q} \text{div} \vec{J}_p + G_p - R_p
\]

\[
\vec{J}_n = q n \mu_n \vec{E}_n + q D_n \nabla n
\]

\[
\vec{J}_p = q p \mu_p \vec{E}_p - q D_p \nabla p
\]
- TFT – Definition of traps(defects) distribution within bandgap
  - Discrete & continuous defects
Low temperature poly: DOS distribution by FE (Field Effect) method

\[ g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \]

\[ g_{TA}(E) = NTA \exp \left[ \frac{E - E_c}{WTA} \right] \]

\[ g_{TD}(E) = NTD \exp \left[ \frac{E - E_v}{WTD} \right] \]

\[ g_{GA}(E) = NGA \exp \left[ -\frac{E - E_{GA}}{WGA} \right]^2 \]

\[ g_{GD}(E) = NGD \exp \left[ -\frac{E - E_{GD}}{WGD} \right]^2 \]
User-defined DOS C-Function

```c
#include <math.h>
#include <stdlib.h>

/*
 * TFT donor trap density as function of energy
 * Statement: DEFECT
 * Parameter: F.TFTDON
 * Arguments:
 * energy   energy relative to valence band (eV)
 * density  tft donor trap density per sqcm
 */
int tftacc(double energy, double *density)
{
    double nta, nda, wta, wda;
    nta = 1e20;
    nda = 2e17;
    wta = 0.025;
    wda = 0.1;

    *density = nta*exp(-energy/wta) + nda*exp(-energy/wda);

    return(0);
}
```
- TFT – Grain boundary defects effects

[Diagram showing energy levels and grain boundary effects]
- TFT's leakage current simulation
  - trap-assisted tunneling with coulombic well
  - band-to-band tunneling

\[
R_{n,SRH} = \frac{P_n - n_{ie}^2}{\frac{TAUN0}{1 + \Gamma_{DIRAC}} \left[ n + n_{ie} \exp\left( \frac{ETRAP}{kT_L} \right) \right] + \frac{TAUN0}{\chi_F + \Gamma_{COUL}} \left[ p + n_{ie} \exp\left( \frac{-ETRAP}{kT_L} \right) \right]}
\]

\[
R_{p,SRH} = \frac{P_n - n_{ie}^2}{\frac{TAUP0}{\chi_F + \Gamma_{COUL}} \left[ n + n_{ie} \exp\left( \frac{ETRAP}{kT_L} \right) \right] + \frac{TAUN0}{1 + \Gamma_{DIRAC}} \left[ p + n_{ie} \exp\left( \frac{-ETRAP}{kT_L} \right) \right]}
\]

\[
G_{BBT} = BB.A \cdot BB.GAMMA \cdot \exp\left( \frac{BB.B}{E} \right)
\]
Mobility Models

Low field mobility

\[ \mu_{n0} = \text{MUN} \left( \frac{T_L}{300} \right)^{-\text{TMUN}} \]

\[ \mu_{p0} = \text{MUP} \left( \frac{T_L}{300} \right)^{-\text{TMUP}} \]

High field mobility – velocity saturation

\[ \mu_n(E) = \mu_{n0} \left[ \frac{1}{1 + \left( \frac{E}{\text{BETAN}} \right)} \right] \]

\[ \mu_p(E) = \mu_{p0} \left[ \frac{1}{1 + \left( \frac{E}{\text{BETAP}} \right)} \right] \]
a-Si TFT Simulation: ATHENA
a-Si TFT Simulation: Transfer Curve
a-Si TFT Device Simulation Example

Back-light leakage current (Photo-generated current by Luminous ray-tracing)
ATLAS – 2D/3D TFT Device Simulation

- poly-Si TFT Device Simulation Example

- Transverse Grain Boundary (Intergrain Interface)
- Top Grain Boundary (Poly-Si/Gate Oxide Interface)
- Poly-Si Gate
- Gate Oxide
- Bottom Grain Boundary (Poly-Si/Buffer Oxide Interface)
- Buffer Oxide
- Grain

- $W_L = 50 \mu m$, $L = 5 \mu m$
- Temperature = 27°C
- $V_{ds} = 5.0V$
- $V_{ds} = 1.0V$
- $V_{ds} = 0.1V$

- Measured $V_{ds} = 0.1V$
- Measured $V_{ds} = 1.0V$
- Measured $V_{ds} = 5.0V$
- Simulated $V_{ds} = 0.1V$
- Simulated $V_{ds} = 1.0V$
- Simulated $V_{ds} = 5.0V$

- Gate voltage ($V_{gs}$) vs. Drain current ($I_{ds}$) characteristics
- Source Current ($I_{source}$) vs. Gate voltage ($V_{gs}$) characteristics
ATLAS – 2D/3D TFT Device Simulation

- Lattice Temperature Distribution & IDVD

![Lattice Temperature Distribution Graph](image)

![IDVD Graph](image)

TCAD for Flat Panel Display

SILVACO
Two approaches to circuit simulation:

- ATLAS Simulation
- Parameter Extraction
- Circuit Simulation
- IV Curve Set
- SPICE Model
- Circuit Performance
- ATLAS Process Structure
- ATLAS/MixedMode Simulation
Typical Pixel Charging and Holding

Driving a pixel and effect of the parasitic capacitance
ATLAS – 2D/3D TFT Device Simulation: TFT-LCD Pixel Simulation

\[ \varepsilon_{ps} = \varepsilon_{pl} + \delta \cdot \gamma \cdot \exp(D_{IMF}) \cdot \sqrt{\frac{V}{V_c}} - 1. \]

\[ C_{lc} = \frac{\varepsilon_0 \cdot \varepsilon_{FS} \cdot L \cdot W}{D} \]
ATLAS – 2D/3D TFT Device Simulation: TFT-LCD
Pixel Simulation

BEGIN

vcom 6 0 5
vg 1 0 20 pulse 0 20 0 1e-9 1e-9 5ms 16.7ms
vd 5 0 10 pulse 0 10 0 1e-9 1e-9 16.7ms 33.4ms
atft 2=source 1=gate 5=drain infile=atft.str width=20
re 2 3 1.28k
co 3 4 317f
#rlc 4 0 10g
#clc 4 0 125f
bLC 4 6 infile=lc_cap.lib function=my_lc_rc
numeric vchange=0.5 imaxdc=200
.options m2ln print
.save outfile=tft_dc
.print
.end
#include <math.h>
#include <stdio.h>

double my_lc_rc(double v, double temp, double ktq, double time,
    double *curr, double *didv, double *cap, double *charge)
{
    double eps,e0;
    double epl,clc;
    double theta,gamma;
    double Dtime;
    double vc;
    double L,W,D;

    L=152;
    W=148;
    Dtime=100e-3;
    theta=51.0; /* sec */
    gamma=51.2e-3; /* sec */
    epl=3.1;
    vc=1.887;
    D=10.02;
    e0 = 8.854e-12;

    if(v > vc)
        eps = epl + theta*gamma*exp(Dtime)*sqrt(v/vc - 1.0);
    else if( v <= vc)
        eps =epl;

    clc= e0*eps*L*W*1e-6/D; /* F */
    *curr=v/10e6;
    *didv=1/10e6;
    *cap=clc;
    *charge=*cap*v;

    /*
     * printf("clc = %e(F)\n", clc);
     * printf("charge = %e\n", *charge);
     */

    return(0);
}
B – User-defined two-terminal element

Syntax

\[ Bxxx \ n+ \ n- \ \text{INFILE}=\text{file}\_name \ \text{FUNCTION}=\text{function}\_name \]

Description

**Bxxx**: User-defined two-terminal element name. It must begin with B.

**n+**, **n-**: Positive and negative terminal nodes.

**INFILE**: Name of the text file (**file\_name**) that contains C source code for a user-defined function that describes element behavior. This file can contain more than one function description.

**function\_name**: Name of the function (**function\_name**) from the file.

Example

```
B1 2 3 infile=ud.c function=rc
```
\[ I = F_1(U, t) + F_2(U, t) \cdot \left( \frac{dU}{dt} \right) \]

- **F_1(U,t):** the DC current.
- **F_2(U,t):** the capacitance.
- **dF_1(U,t)/dU:** the DC differential conductance.
- **Q:** the charge associated with F_2(U,t).
**Input Parameters**

Four input parameters are supplied to the function and can be used in the user-defined code. The input parameters are:

- $v$: the voltage across the element (V)
- $\text{temp}$: the temperature (K)
- $ktq$: the thermal voltage $kT/q$ (V)
- $\text{time}$: transient time (sec); a value of 0 is supplied during DC calculations

**Output Parameters**

The four output parameters that must be returned by the function are:

- $\text{curr}$: the value of $F1$ (Amps)
- $\text{didv}$: the value of $dF1(v, \text{time})/dU$ (A/V)
- $\text{cap}$: the value of $F2(v, \text{time})$
- $\text{charge}$: the value of the charge (Q)
$I(U, t) = \frac{U}{R} + C \cdot \left( \frac{dU}{dt} \right)$

$F1(U, t) = \frac{U}{R}$

$F2(U, t) = C$

$\frac{dF(U, t)}{dU} = \frac{1}{R}$

$Q = C \cdot U$

When $R=2\,\Omega$ and $C=100\,\text{pF}$, a user-defined function could have the following form:

```c
intrc(double v, double temp, double ktq, double time, double *curr, double *didv, double *cap, double *charge)
{
    *curr = v/2000.0;
    *didv = 1.0/2000.0
    *cap = 1.0e-10;
    *charge=1.0e-10*v;
    return(0); /* 0 - ok */
}
```
ATLAS – 2D/3D TFT Device Simulation: Backlight Effects Using MixedMode

- MixedMode – TFT device + Spice circuit
- Backlight Effect
ATLAS – 2D/3D TFT Device Simulation: ESD Simulation Using MixedMode+Giga

- ESD Simulation: Mixedmode + Giga (lattice temperature)

Ex) Diode ESD: CDM model

[Diagram of ESD protection device]
Transport Mechanisms

- **Metal & Semiconductors**: charge transport are limited by scattering of the carriers, mainly due to thermally induced lattice deformations and phonons. Transport is limited by phonon scattering. Charge mobility decreases with temperature.

- **Organic materials**: transport occurs by phonon assisted hopping of charges between localized states. Charge mobility increases with temperature.

- General mobility model of organic material including Poole-Frenkel field-dependent mobility.
EL mechanism & Organic Models
- Charge Injection (metal contact)
  - Ohmic (Dirichlet boundary condition)
  - Schottky contact (injection limited current):
    - thermionic emission model - tunneling
    - interface barrier lowering
- Transport model (bulk)
  - space-charge-limited current: Poisson + Current continuity equations
  - trap-charge-limited current: DDM + Defects states
- Hopping process: Poole-Frenkel mobility
- Recombination & Emission (internal efficiency)
  - Langevin radiative recombination
  - Exiton radiative decay – singlets/triplets (1 FL:3 PL default)
- Optical Output Coupling calculation

\[
R_{np} = \frac{n_e n_p}{\varepsilon_{eo}} (\mu_n(E) + \mu_p(E))
\]

\[
\frac{dS(x,t)}{dt} = \gamma r(x,t)n(x,t)p(x,t) + D_s \frac{d^2 S(x,t)}{dx^2} \frac{S(x,t)}{\tau}.
\]
ATLAS – 2D/3D TFT Devices Simulation: OTFT/OLED – Organic Devices Simulation
Metal/Organic Interface injection

I.D. Parker J.Appl. Phys. 75(3), 1 Feb 1994, p.1656
- Cathode injection
- Cathode Ca(2.9eV)

I.D. Parker J.Appl. Phys. 75(3), 1 Feb 1994, p.1656
Bilayer TPD/Alq3 OLED Example: Exciton Density & Profile
Bilayer TPD/Alq3 OLED Example: IL & Internal Efficiency
ATLAS – 2D/3D TFT Devices Simulation: OTFT/OLED – Organic Devices Simulation

- Bilayer TPD/Alq3 OLED Example: IL & Internal Efficiency

Fig. 14. The light emission from a typical OLED device can be divided into three types of modes shown in this figure. External modes that are able to escape through the surface, and two waveguide modes, which are either trapped in the substrate or in the organic/ITO layers of the device.

\[ \eta_{\text{ext}} = \gamma \times r_{\text{st}} \times q \times \eta_{\text{coupling}} \]
Bilayer TPD/Alq3 OLED Example: Optical output Coupling & External Efficiency
Spice Back Annotation Flow For TFT Design

- **LAYOUT**
  - Device extraction (MOS Tr, TFT Tr)
  - LPE (RC extraction)

- **Celebrity**
  - Discovery
  - CLEVER

- **SmartSpice**
  - Liquid crystal modeling
  - Spice TFT model poly, a-si (RPI)
  - Spice Simulation

- **EXPERT**
  - Verilog-A
  - SmartSpice
Clever - 3D Field Solver for Parasitic RC Extraction

- Based on 3D Structure by layout(gds), Clever 3D field solver is very accurate and powerful!
Clever - 3D Field Solver for Parasitic RC Extraction: Extracted Spice Netlist

M1 int1 int2 int0 GND TFT w=1u l=1u As=8.125p Ad=1.25p Ps=18.0355u Pd=4.5u Nrs=0 Nrd=0.5 geo=0
M2 int1 int4 int3 GND TFT w=1u l=1u As=8.125p Ad=1.25p Ps=18.0355u Pd=4.5u Nrs=0 Nrd=0.5 geo=0
M3 int1 int6 int5 GND TFT w=1u l=1u As=8.125p Ad=1.25p Ps=18.0355u Pd=4.5u Nrs=0 Nrd=0.5 geo=0
M4 int7 int8 int7 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
M5 int7 int9 int7 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
M6 int7 int10 int7 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
M7 int11 int12 int11 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
M8 int11 gate7 int11 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
M9 int11 int14 int11 GND TFT w=1u l=1u As=15.2875p Ad=1.25p Ps=30.3196u Pd=4.5u Nrs=8.75 Nrd=0.5 geo=0
C1 gate7 SL4_0 1.0526754e-15
C2 gate7 SL3_0 2.4251317e-15
C3 gate7 SL2_0 2.4296517e-15
C4 gate7 PG1_B_1 6.8366726e-16
C5 gate7 PG3_1 8.1596645e-16
C6 gate7 PG2_B_1 2.5646589e-15
C7 gate7 ITO_3_0 1.4105912e-15
C8 gate7 PG3_B_0 3.8891131e-18
C9 gate7 GND 6.1081757e-16

Parasitic netlist

Active Tr.
What is modeled?

Capacitance of LC

Modeling of Liquid-Crystal’s Capacitance

- 47 -
Capacitance Modeling

\[ C = \hat{e}_0 \hat{e}_\varepsilon \frac{L[W]}{d} \]

\[ \Phi_r = \Phi_{pi} + f_A f_A e^{D \cdot t} \cdot \sqrt{\frac{V}{V_c}} \]


```
// Capacitor model
#include "discipline.h"
#include "Constants.h"
module capacitor(p,n);
  electrical p,n;
  parameter real c0=1e-15;
analog
  begin
    if( V(p) == V(n) )
      t1=$realtime;
    @( cross( V(p)-V(n),+1 ))
      t2=$realtime-t1;
    vpn=V(p)/V(n)-1;
    tp=sqrt(vpn);
    er=ep+delta*gamma*exp(k*t2)*tp;
    I(cap) <+ ddt(c0*er*V(cap));
  end
endmodule
```
Summary

- ATHENA
  - TFT Device Process and Topography Simulation

- ATLAS
  - SPIESCES+TFT: TFT Electrical Characteristics by DOS
  - Luminous: ray-tracing back-light leakage current analysis
  - OTFT: Organic TFT
  - OLED: Organic LED
  - MixedMode: TFT-LCD Pixel Simulation (LC cap model)
  - Giga+MixedMode: ESD(CDM,HBM,MM)

- CLEVER
  - Pixel’s Parasitic RC Extraction by accurate 3D Field Solver
  - Back annotated spice netlist extraction

- SmartSpice:Verilog-A
  - LC cap. Modeling